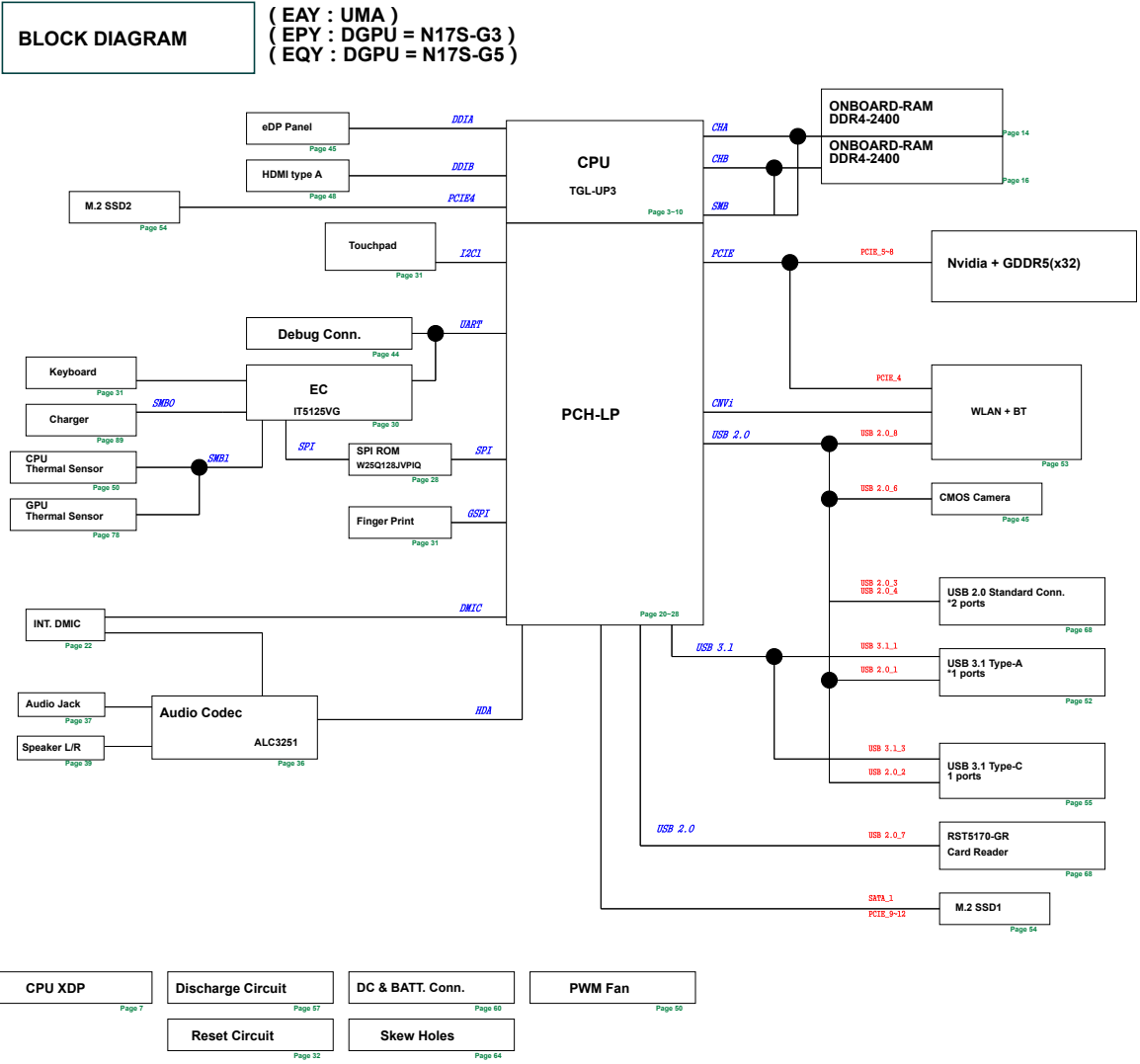


X421 SCHEMATIC Revision 1.0

SYSTEM PAGE REF.	
PAGE	Content
1	Block Diagram
2	SKU Table
3	CPU_DISPLAY
4	CPU_DDR4
5	CPU_LFC,ESPI,SPI,SMB,CLINK
6	CPU_POEWR
8	CPU_MISC,UTAG
9	CPU_CFG,RSVD
10	CPU_POWER_CAP
13	DDR4_TERMINATION
14	DDR4_ON-BOARD_A(1)
16	DDR4_ON-BOARD_B(1)
19	DDR4_CA_DQ_VOLTAGE
20	CPU_FCH_CSI2,CNV1
21	CPU_FCH_GSPI,I2C,UART,ISH
22	CPU_FCH_AUDIO,SNDR
23	CPU_FCH_PCIE,USB,SATA
24	CPU_FCH_CLOCK SIGNALS,RTC
25	CPU_FCH_SYS_POWER
26	CPU_FCH_POEWR
27	CPU_FCH_POEWR,GND
28	FCH-SPI ROM,OTH
29	TEST_POINT
30	KBC_IT5125VG_ICE
31	KBC_KB,TP,KB-light
32	RESET Circuit
36	AUD_CODEC ALC3251
37	AUD-JACK
39	AUD-SPEAKER CONNECTOR
40	Card Reader AU6465
44	BUG_Debug
45	eDP_LCD_Camera_MIC
48	HDMI-type A
50	FAN_Thermal Sensor
52	USB30
53	USB Port
54	NGFF(KEY-E)_WLAN
55	NGFF(KEY-M)_SSD
57	TypeC_CONN&CC logic
58	DSG_Discharge
59	PRO_PROTECT
60	Power Switch
64	DC_DC & BAT IN
68	ME_Conn & Skew Hole
69	B to B connector
70	VGA_nVIDIA_N17S_PCIE
71	VGA_nVIDIA_N17S_FB-IF
72	VGA_NV_N17S_FB-GDDR5
73	VGA_nVIDIA_N17S_VDD
74	VGA_nVIDIA_N17S_DISPLAY
75	VGA_nVIDIA_N17S_XTAL
76	VGA_nVIDIA_N17S_GPIO
77	VGA_nVIDIA_N17S_POWER
78	Thermal_PROTECTION
79	VGA_Sequence

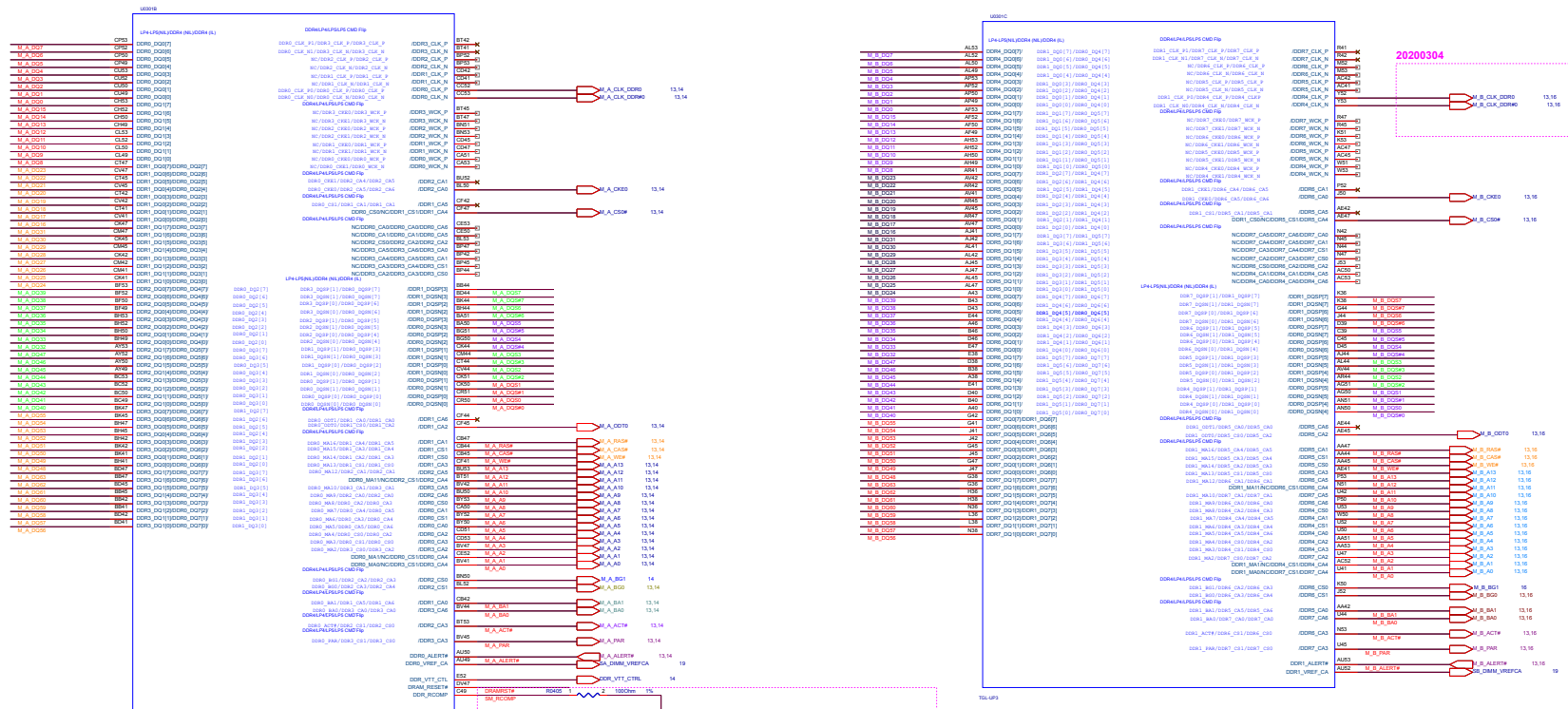
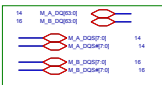


Power

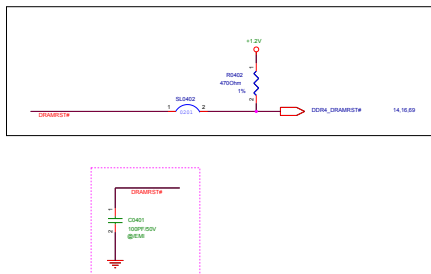
- PW_IMVP9 (Page 80-82)
- +3VADSW/+5VSUS (Page 87)
- +1.8VSUS (Page 83)
- +1.2V / +VTT / +2.5V (Page 86)
- +NVVDD (Page 91)
- +FBVDDQ/+PEX_VDD (Page 93)
- Charger (Page 89)
- Load Switch (Page 88)

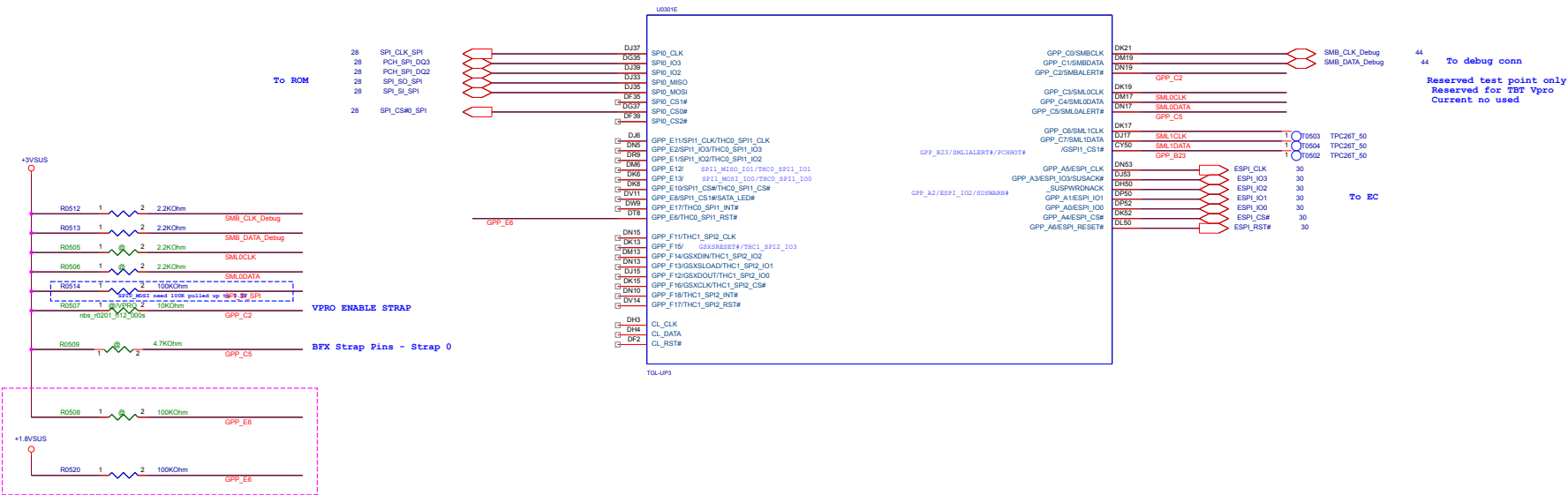


Non-Interleaved



DDR4 COMPENSATION SIGNALS
609003 TGL U DDR4 SODIMM RVP CRB SCH REV0p8

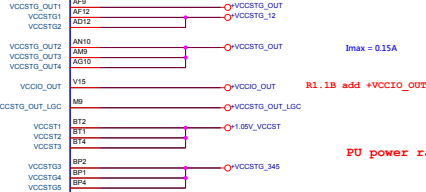
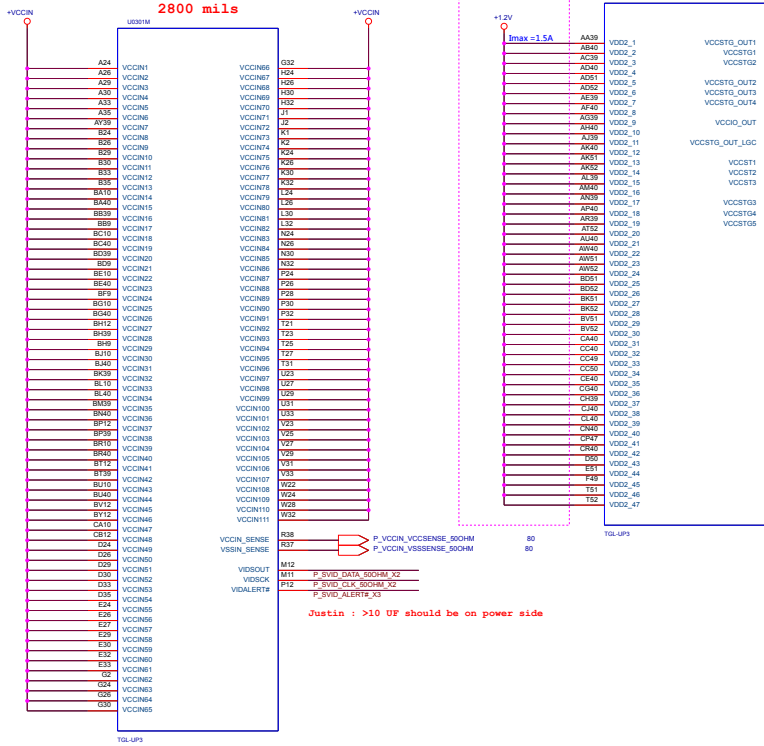




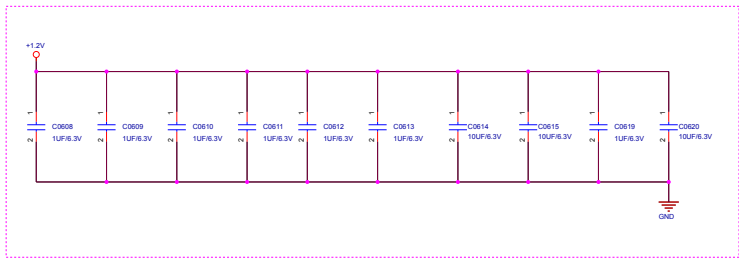
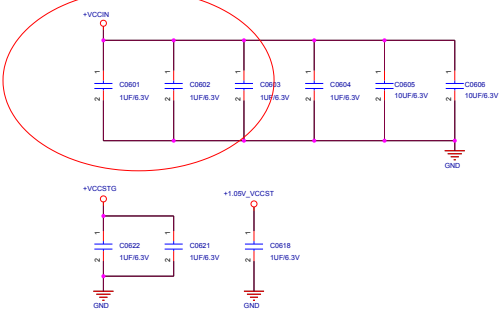
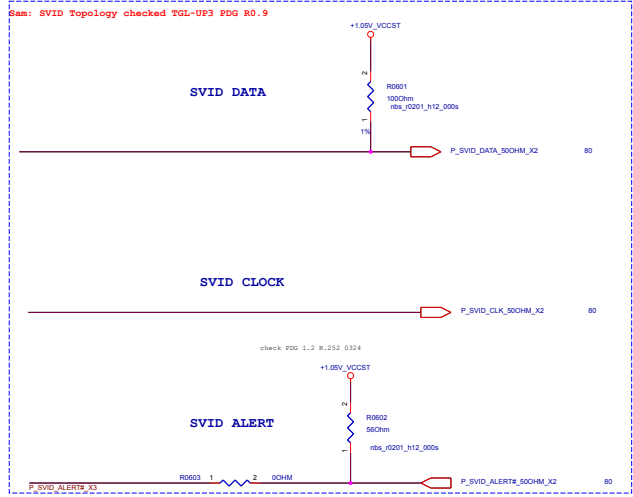
I_{max} = 70A

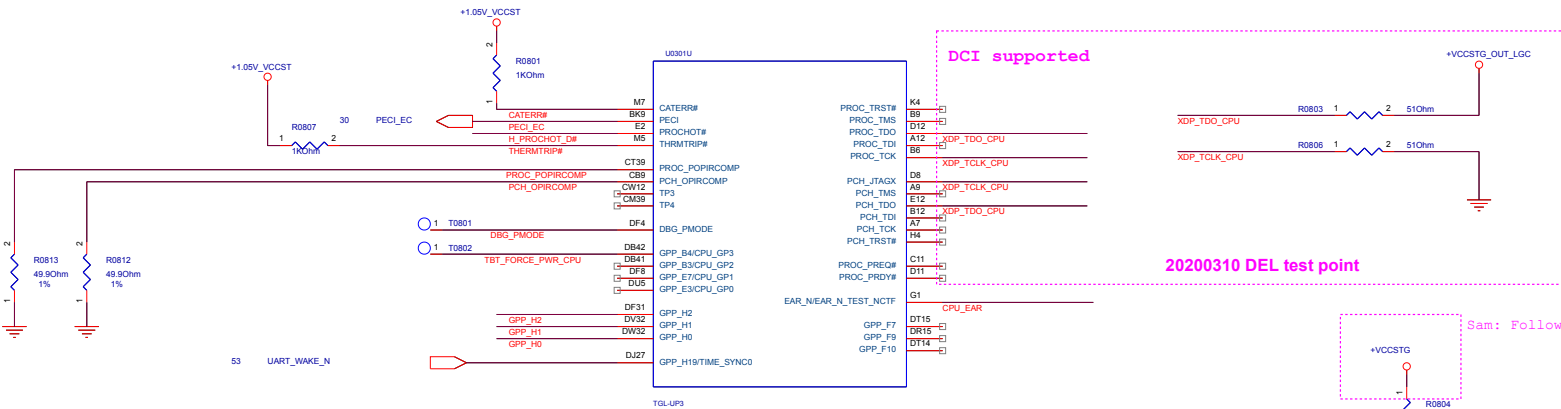
Sam: VDD is +1.2V for DDR4.

2800 mils

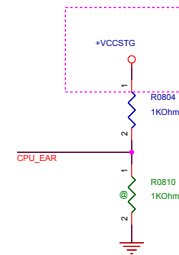


Sam: Follow INTEL TGL-U DDR4 RVP.





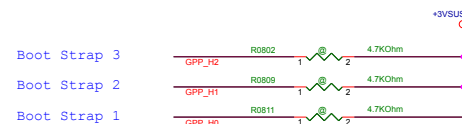
Sam: Follow TGL PDG



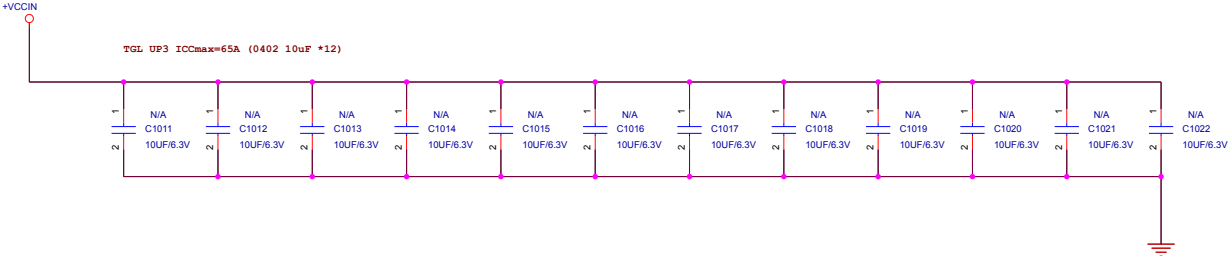
CPU SIDEBAND SIGNALS



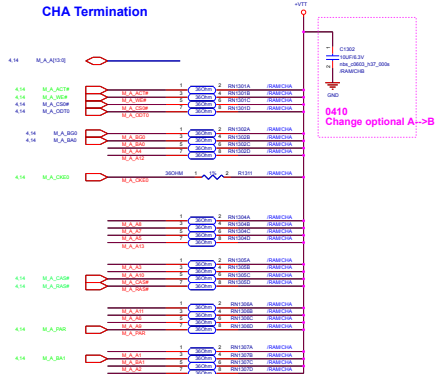
BFX Strap Pins (20 kohm Internal PD)



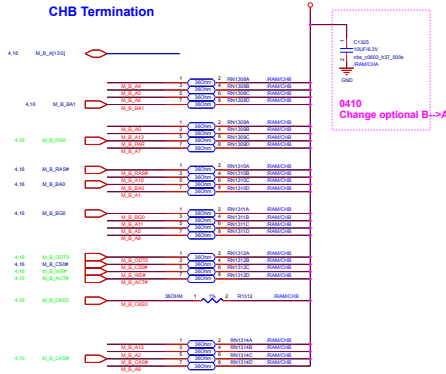
CPU - VCCIN DECAPS- Underneath the package



CHA Termination



CHB Termination

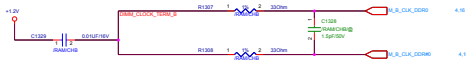


CHA CLK Termination



C1301 and C1328 Close to CPU

CHB CLK Termination



CHA BG1 Rtt for DDP.



R1309 is installed for DDP

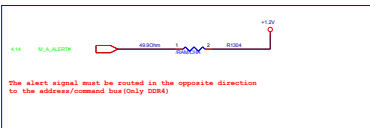
refw to #576715_MHLS_U_DDR4_HDR_CORE_Sch_Rev1p0 Page45

CHB BG1 Rtt for DDP.

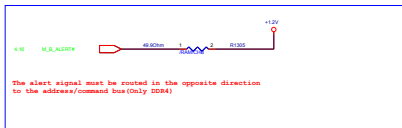


R1310 is installed for DDP

refw to #576715_MHLS_U_DDR4_HDR_CORE_Sch_Rev1p0 Page46



The alert signal must be routed in the opposite direction to the address/command bus(Only DDR4)



The alert signal must be routed in the opposite direction to the address/command bus(Only DDR4)

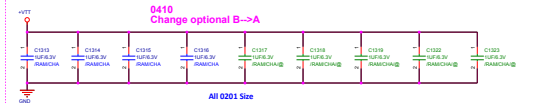
0410 Change optional A->B



All 0201 Size

C1305 Close to RN1301 / RN1302
C1306 Close to RN1303 / RN1304
C1307 Close to RN1305 / RN1306
C1308 Close to RN1307 / R1304

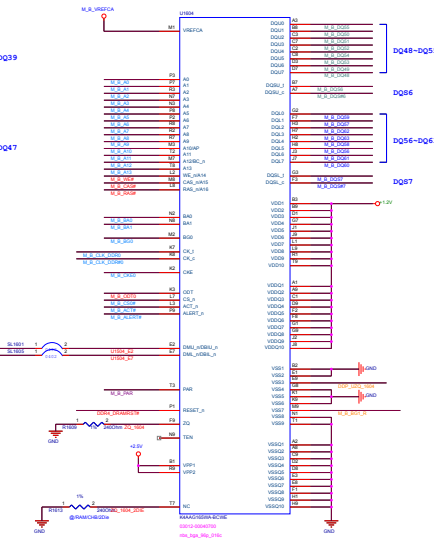
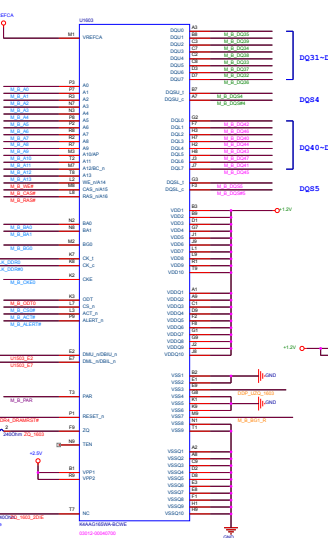
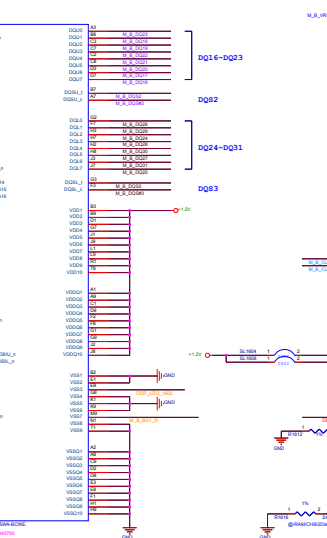
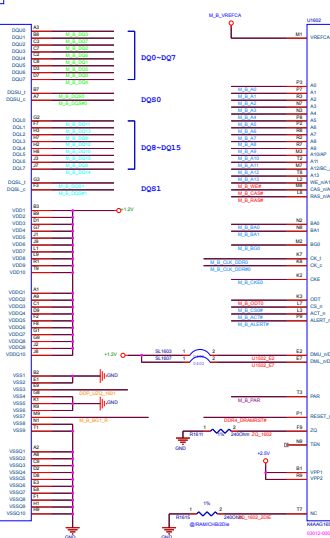
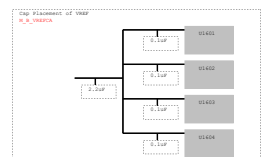
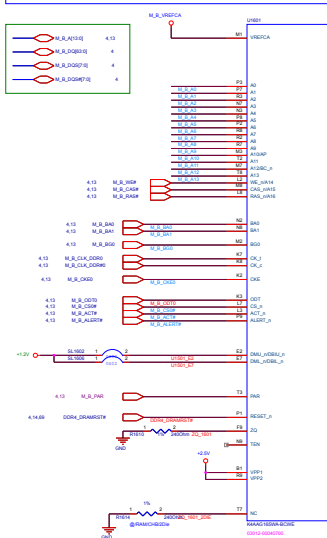
0410 Change optional B->A



All 0201 Size

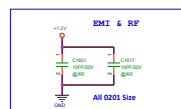
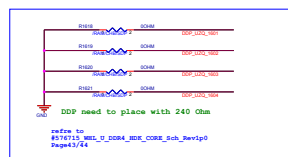
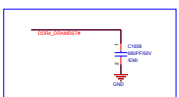
C1313 Close to RN1308 / RN1309
C1314 Close to RN1310 / RN1311
C1315 Close to RN1312 / RN1313
C1316 Close to RN1314 / R1305

DDR4 Pin	SDP	DDP
Pin E9 (U2Q)	GND	240 Ohm PD to GND
Pin M9 (BGI)	GND	BGI signal from Controller

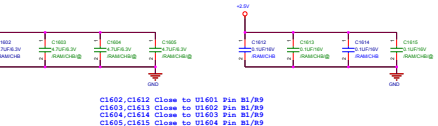


06/12

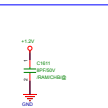
DCR4 DMC/DML Tie all DRAMs DMC0 and DML0 balls directly to VDDQ
refere to #576715_WRL_U_DCR4_0_DDR_CDRR_Sch_Revip0.pdf page42
#575412_WRL_U_SchChecklist_Revip0 Page 15



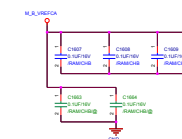
VPP Power



C1602,C1612 Close to U1601 Pin B1/R9
C1603,C1613 Close to U1602 Pin B1/R9
C1604,C1614 Close to U1603 Pin B1/R9
C1605,C1615 Close to U1604 Pin B1/R9



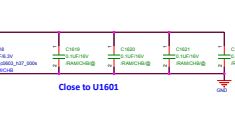
VREFCA Power



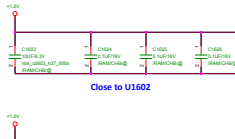
```
C1607/C1663 Close to U1601 Pin M1
C1608/C1664 Close to U1602 Pin M1
C1609 Close to U1603 Pin M1
C1610 Close to U1604 Pin M1

08/23 Add C1663/C1664 0.1UF/16V
```

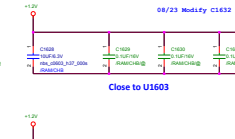
VDD/VDDQ Power



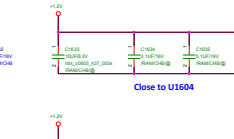
All 0201 Size



All 0201 Size



All 0201 Size

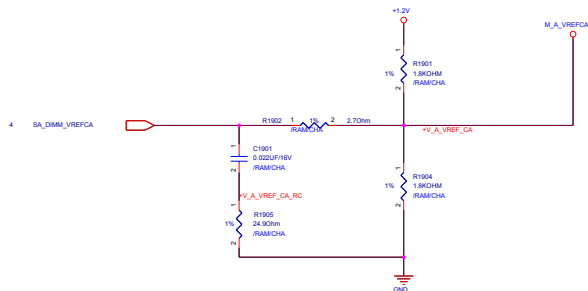


C1855
 10F6.3V
 RAMODdy

All 0201 Size
 Close to U1504

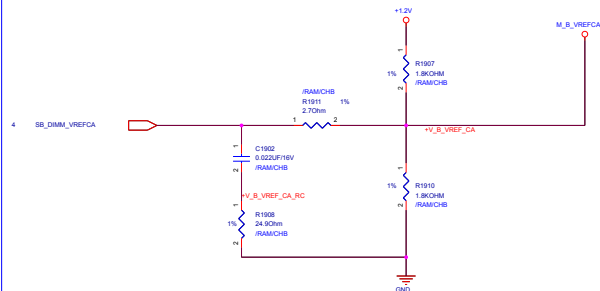
08/23 Modify C1632 to stuff

For DDR4 CHA Vref_CA



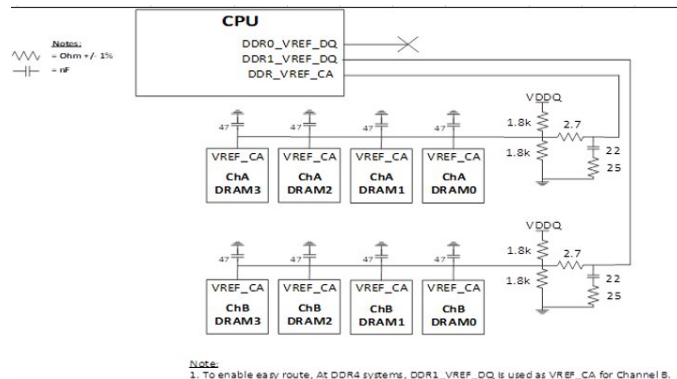
Close to U1401/U1402/U1403/U1404

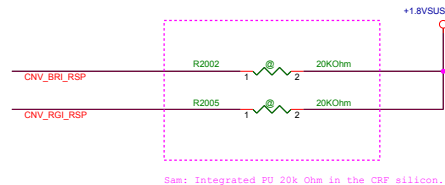
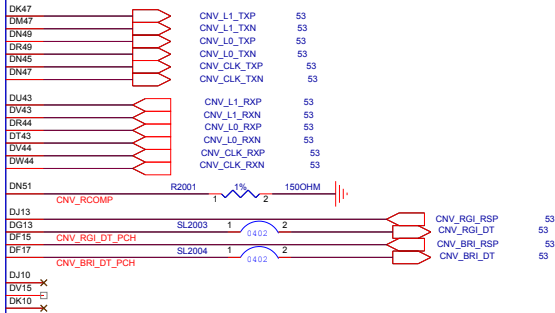
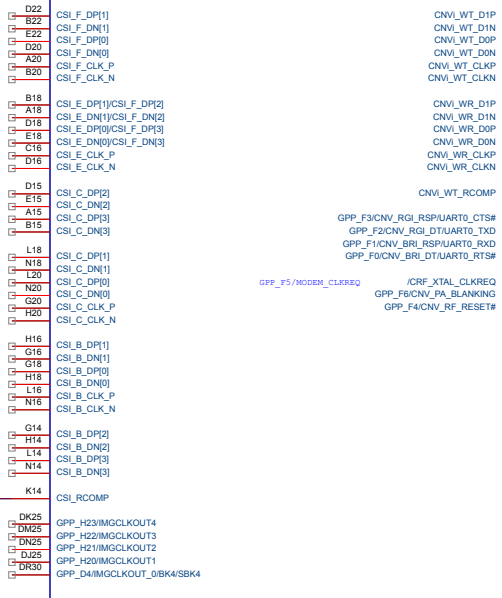
For DDR4 CHB Vref_CA



Close to U1601/U1602/U1603/U1604

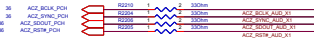
TGL-UP3 DDR4 MD x16





HD Audio

Justin : Either 1.8V or 3.3V used same 33ohm series resistor



Sam : BT_ON changes to GPIO GPP_A13 which follows INTEL TGL CRB.



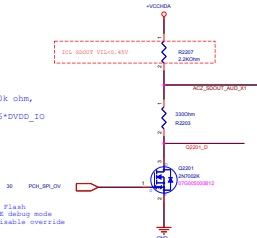
Justin : clkreq0 still need for CMV1 sequence, even if CMV clk is no required on PCH

FLASH DESCRIPTOR STRAP

VCCHDA=+1.8VSUS

HDA_SDO
0=Enable
1=Disable Override

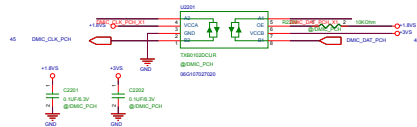
ACZ_SDOOT:(1)ICL PCH: Internal PD 20k ohm,
VIL=0.25*VCC, VIH=0.75*VCC
(2) ALC3288:VIL<0.4*DVDD_IO, VIH>0.6*DVDD_IO

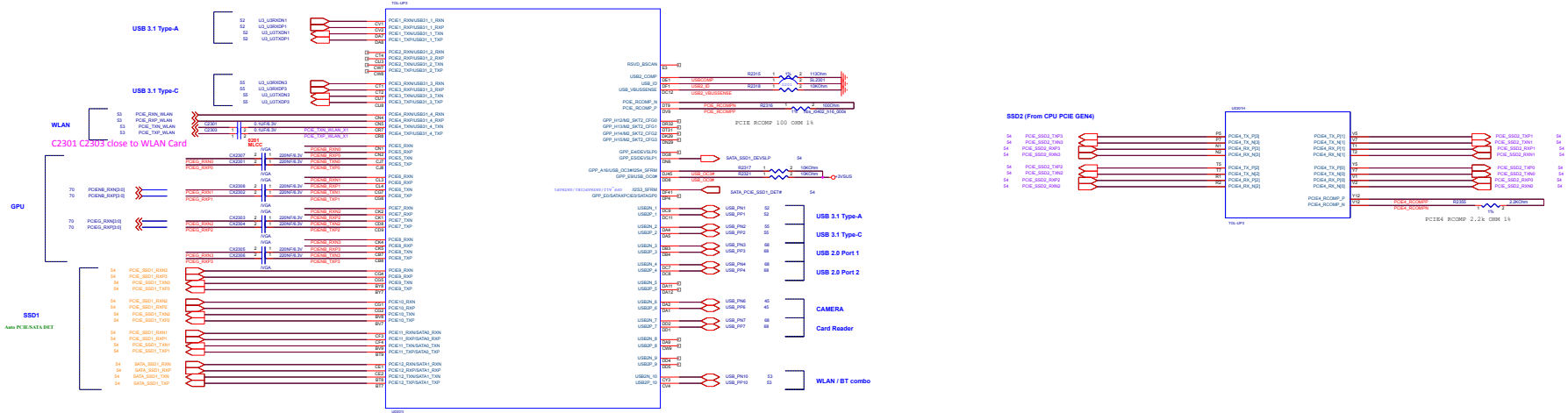


ACZ_SDOOT is a signal used for Flash
Descriptor security Override/ME debug mode
HIGH : get overrideen, LOW : disable override

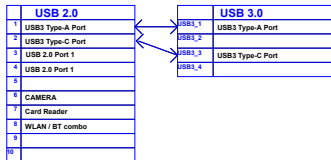
Intel: To enable Flash Descriptor Security Override, this
signal should be pulled up to VCCHDA through a 1
KΩ to 2.2 KΩ ±5% resistor.

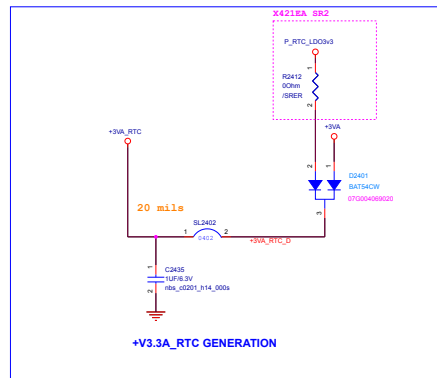
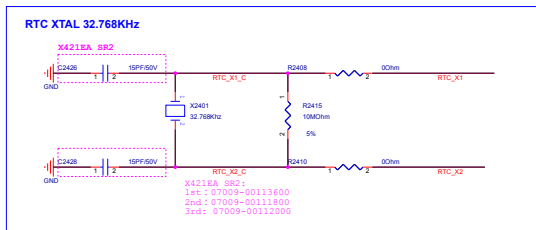
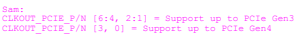
Sam: For TGL, GPP 3 group uses 1.8V only.



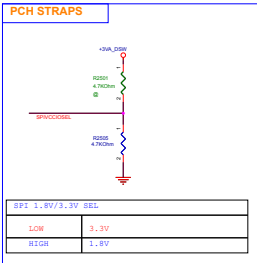
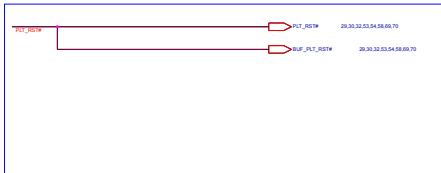
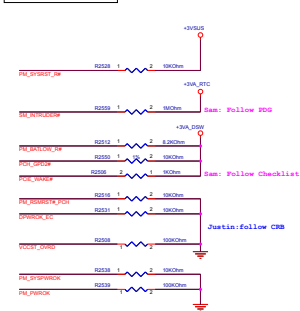
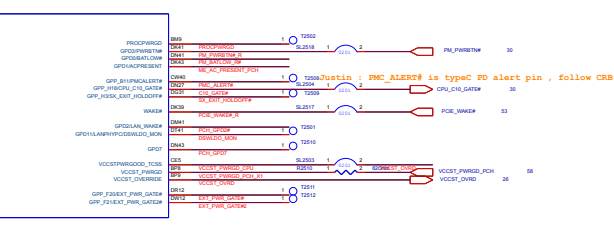


PCI-E* X1	PCI-E USAGE DEFAULT/OPTION	Co-Lay	Clock
PCI-E 1/0/0/0/1-0	N/A		
PCI-E 2/0/0/0/1-0	N/A		
PCI-E 3/0/0/0/1-0	N/A		
PCI-E 4/0/0/0/1-0	N/A		
PCI-E 5	N/A		
PCI-E 6	N/A		
PCI-E 7	N/A		
PCI-E 8	N/A		
PCI-E 9	N/A		
PCI-E 10	N/A		
PCI-E 11/0/0/0/1-0	N/A		
PCI-E 12/0/0/0/1-0	N/A		

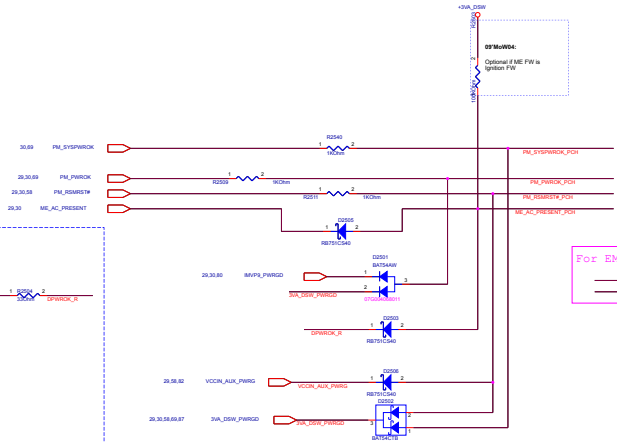
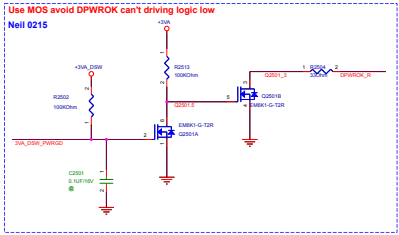




Justin : No used divided resistors, PCH has Rload inside and +3VA PU will cause VCCRTC drop to 2.7V in S0
VCCRTC must not exceed 3.3V and sustained operation at voltages below 3.0V is not recommended
Intel suggested to use diode circuit for long life reliability

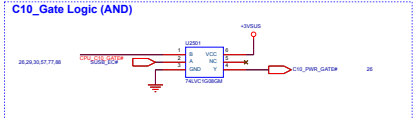


Justin : change to logic IC



For EMI

PM_PWRDK_PCH	00
PM_SYSPWRDK_PCH	00



Power failure solution (S0-->G3,S5-->G3):

Justin : take DSW PWROK low on emergency power loss, it must also take RSMRST# low at the same time

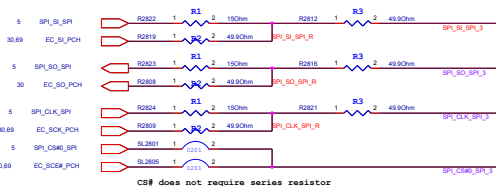
The diagram illustrates a 16-bit parallel adder circuit. It consists of two 74181 ALU chips and a 74160 counter. The 74181 ALU chip is a 16-bit parallel adder with 16 inputs (A0-A15, B0-B15, C0-C15) and 4 outputs (F0-F3). The 74160 counter is a 16-bit parallel counter with 16 inputs (A0-A15) and 4 outputs (F0-F3). The diagram shows how the 74181 ALU chips are interconnected to perform a 16-bit addition, with the 74160 counter providing the carry-in for the adder. The diagram is a detailed schematic of a 16-bit parallel adder using two 74181 ALU chips and a 74160 counter.

SPI PCH Power

Sam : For non-PD system using +3V5US



1-Load Branch Topology (Device Down) with EC Wired-OR Flash Sharing
(Sam: 607872_TGL_UP3_PDG_Rev0p9)

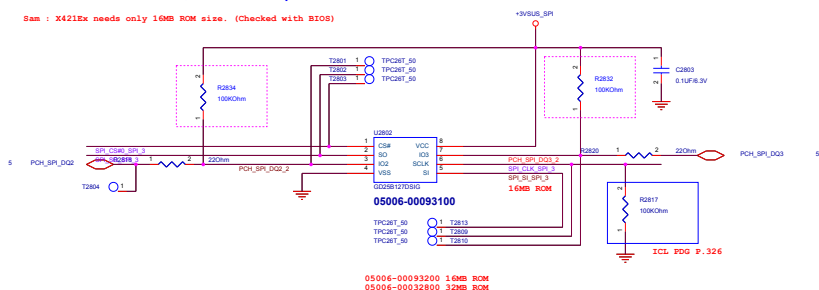


CS# does not require series resistor

PCH SPI ROM 32M/16M Co-lay

Sam : X421Ex needs only 16MB ROM size. (Checked with BIOS)

0324
Change SPI ROM P/M (05006-00093200 --> 05006-00093100)



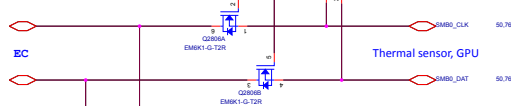
System Management Interface

+3VA_EC

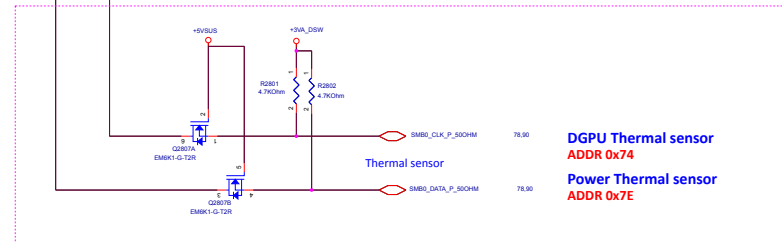
30.60.89 P_SMB0_CLK_50CHM

30.60.89 P_SMB0_DATA_50CHM

EC



CPU Thermal sensor
ADDR 0x91



DGPU Thermal sensor
ADDR 0x74

Power Thermal sensor
ADDR 0x7E

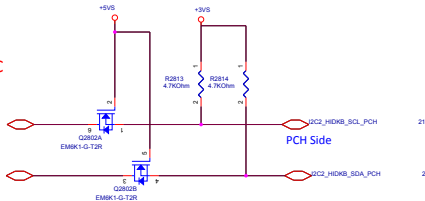
X421EA R1.2: Avoid +5VSUS leakage issue.

+3VA_EC

30 SMB2_CLK

EC

30 SMB2_DAT

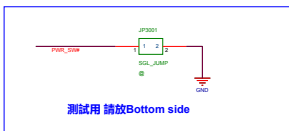


Type-C/Audio debug
TBD

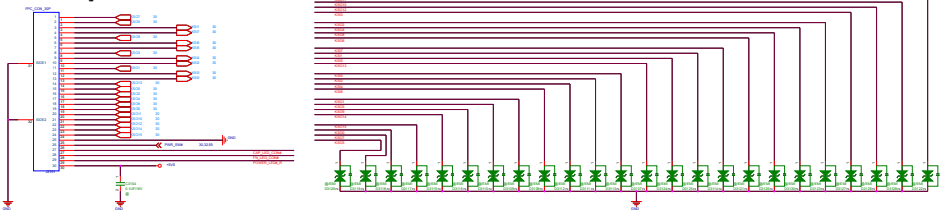
```

ITE5125 GPO2 need pull down for EC load code
      R3010 1 2 2 2 77KOhm

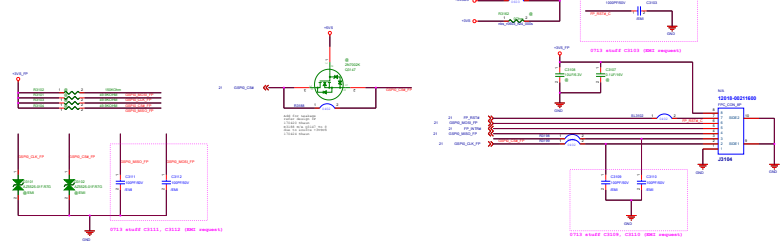
```



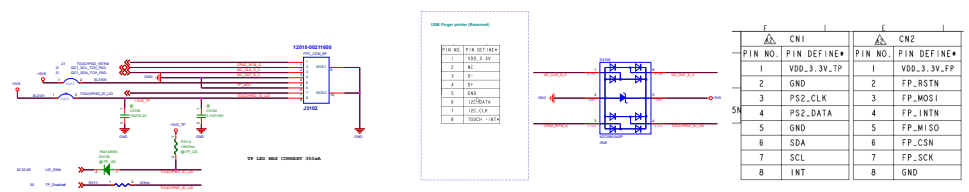
Internal Keyboard



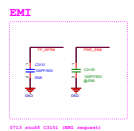
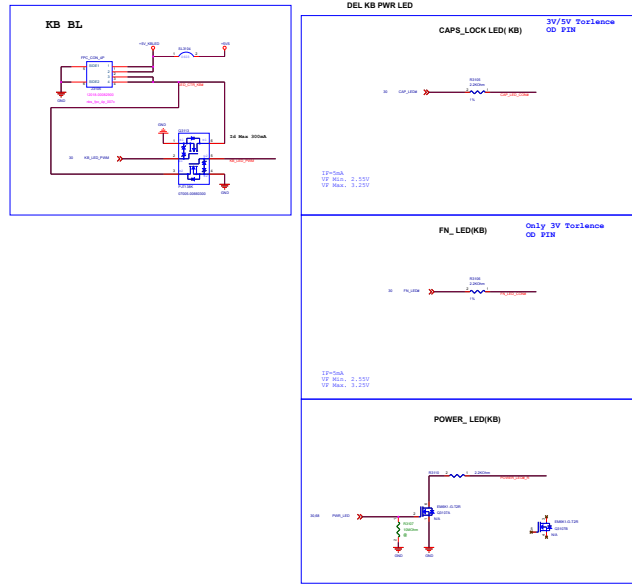
FingerPrint Connector

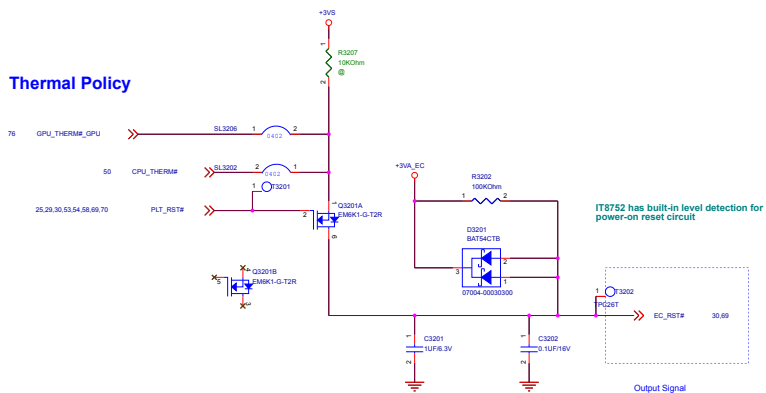


TouchPad Connector

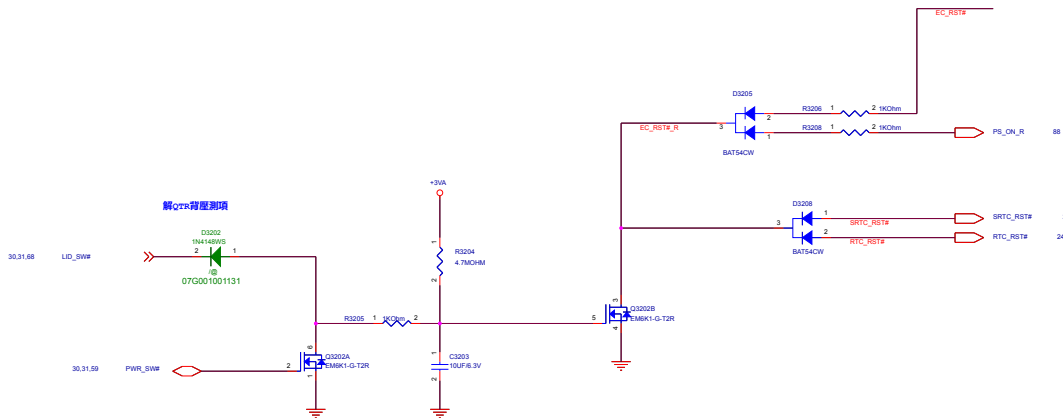


KB Function LEDs



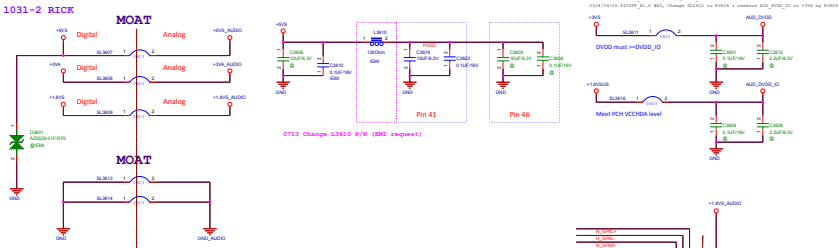


battery embedded (press pwr_sw 10sec, then reset ec)

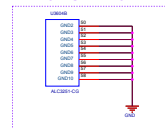


Audio Cdeco ALC3251

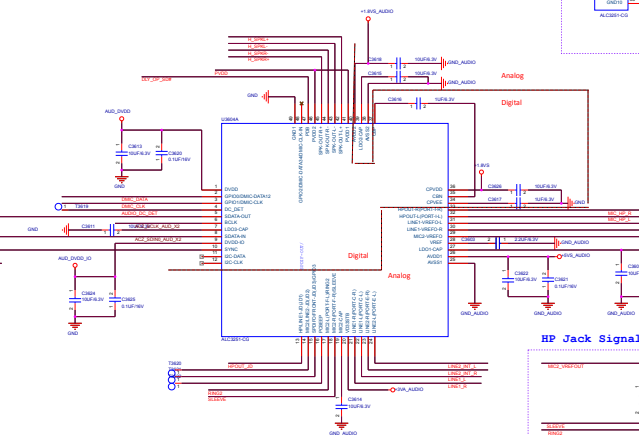
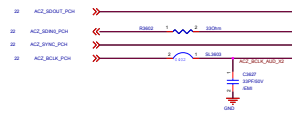
1031-2 RICK



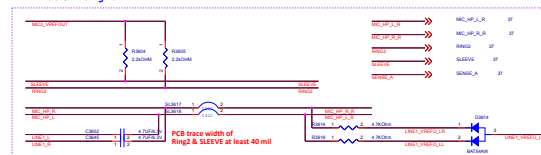
For GND Via



TO SPEAKER CONN.



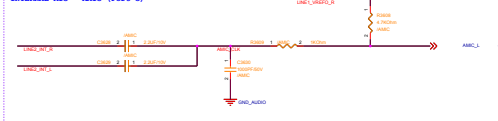
HP Jack Signal



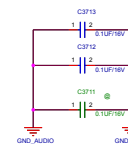
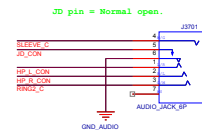
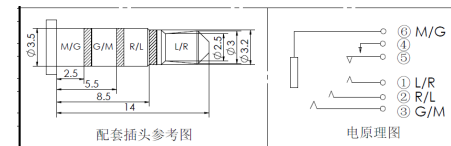
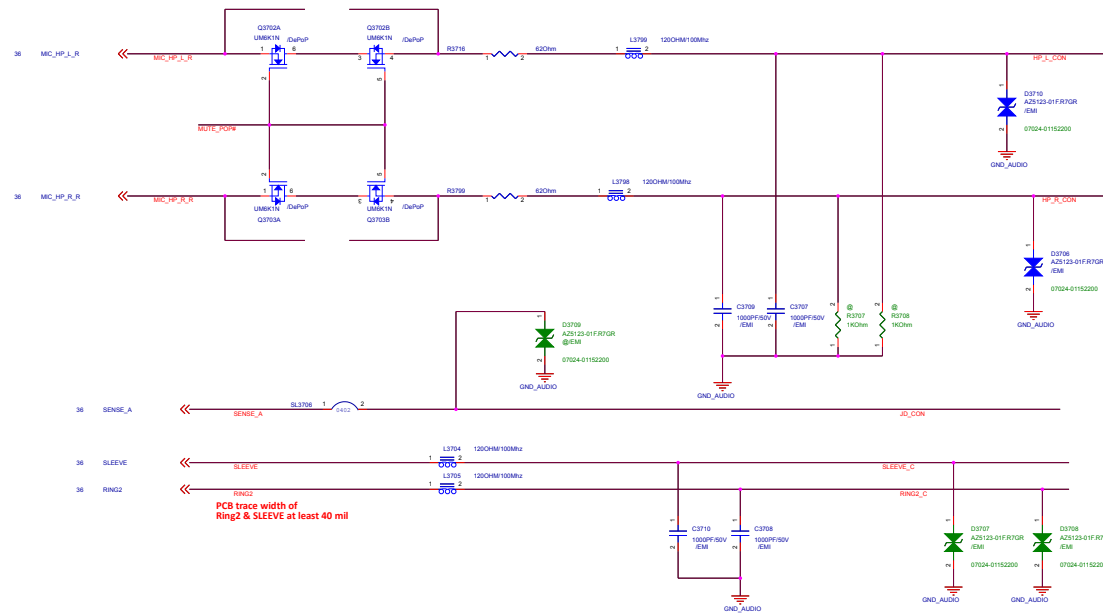
Detection



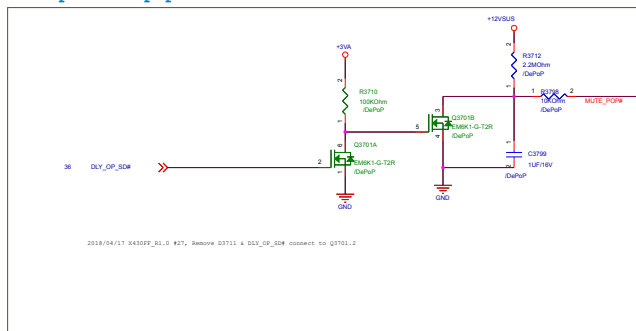
INTERNAL MIC - AMIC (Port C)



Audio Jack



Headphone depop circuit



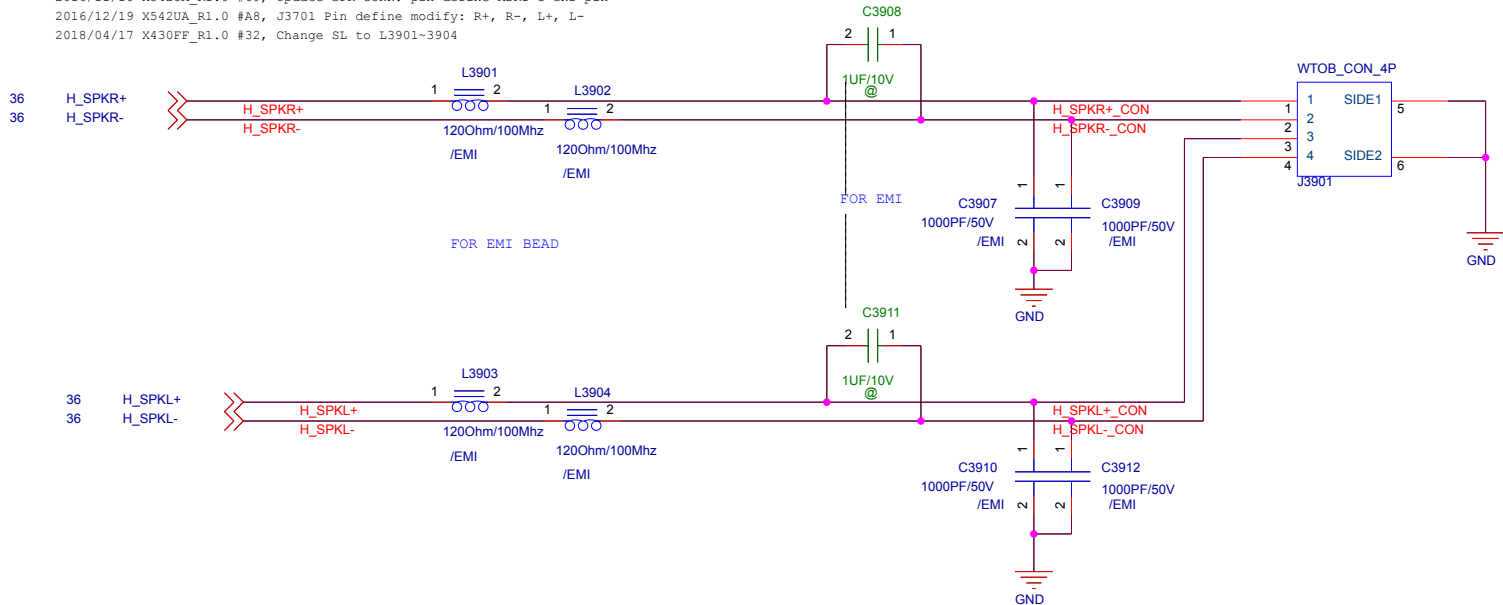
Audio Speaker

Max = 4W / Channel
I = 0.7 A (@Speaker : 8 Ohm)

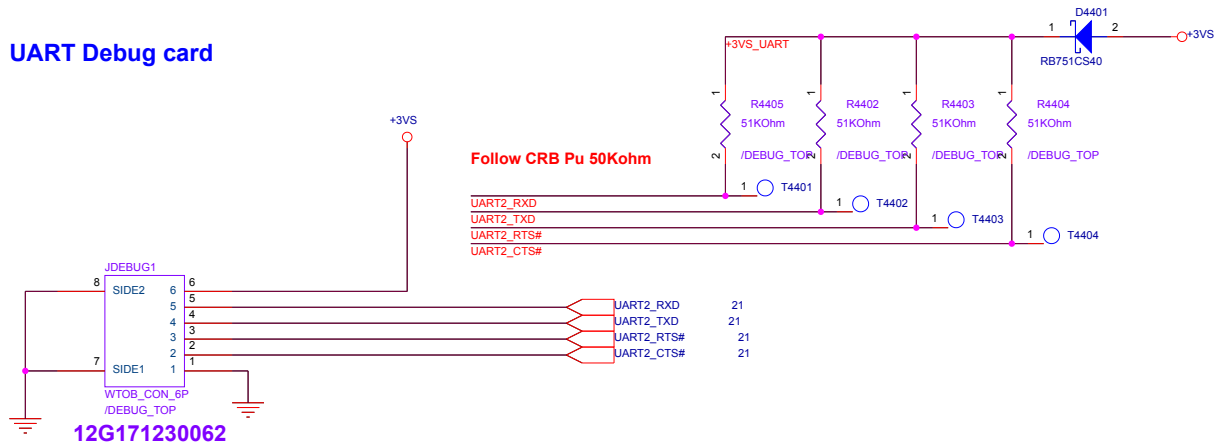
SPK L+ L- R+ R- trace width
Speaker 4 ohm ==> 60mils

INTERNAL SPK Conn.

2016/11/10 X542UA_R1.0 #69, Update SPK CONN. pin define ADRL & GND pin
2016/12/19 X542UA_R1.0 #A8, J3701 Pin define modify: R+, R-, L+, L-
2018/04/17 X430FF_R1.0 #32, Change SL to L3901~3904



UART Debug card

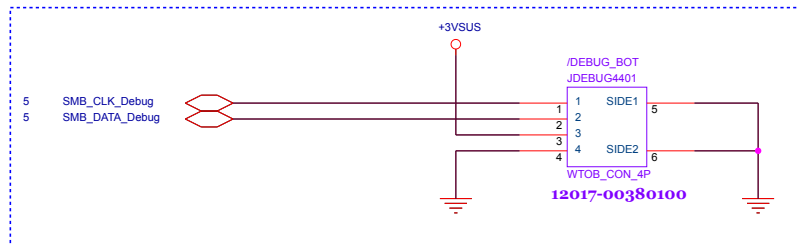


Jigboard4 debug guide

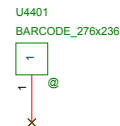
DIP SW to 0000 : BIOS Flash

DIP SW to 0010 : Keyboard CONN Port80

DIP SW to 1000 : SMBUS CONN Port80 & BIOS DUMP(by Postcode monitor)

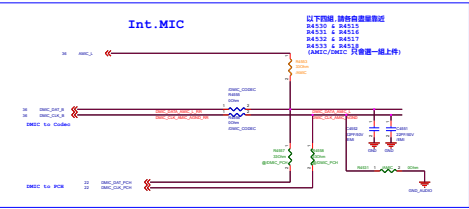
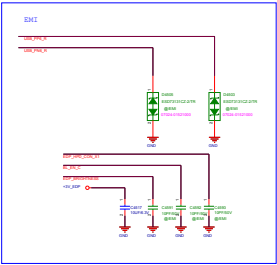
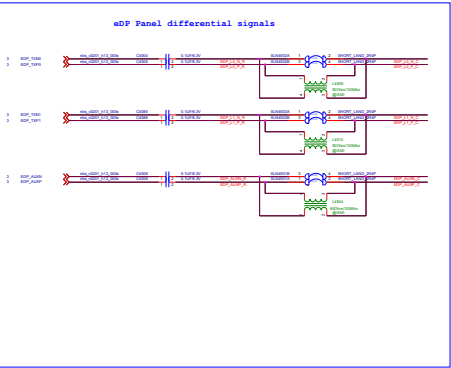
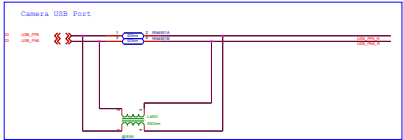
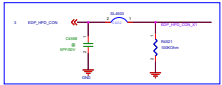
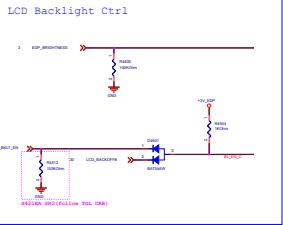
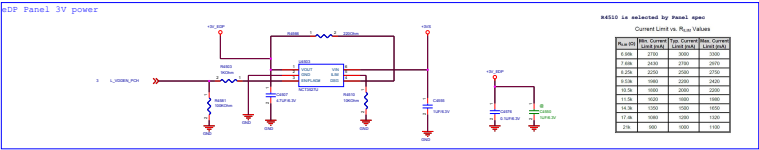


Barcode for EMS

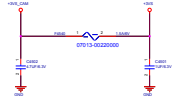


DIMM Debug Port

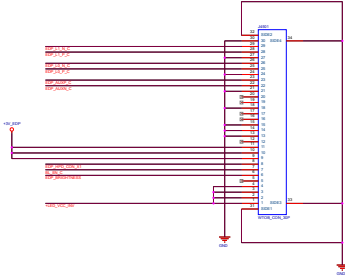
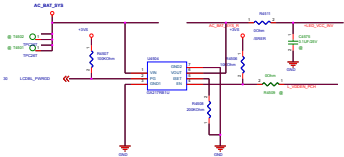
eDP Panel



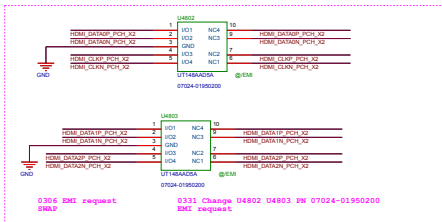
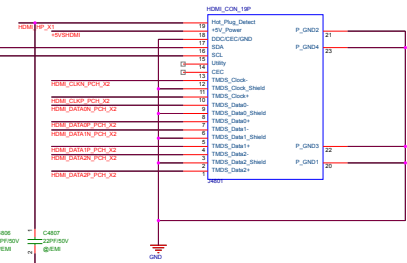
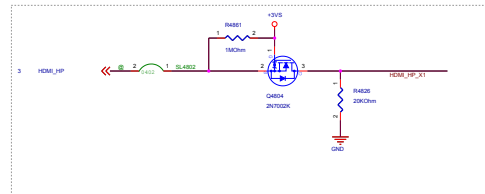
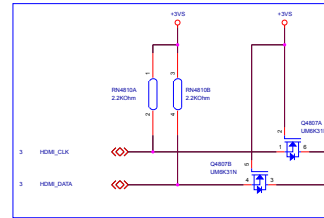
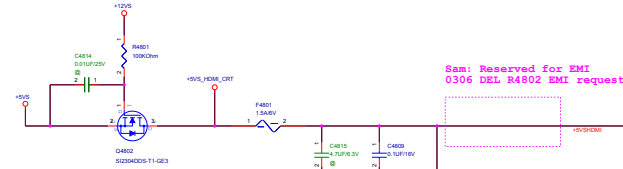
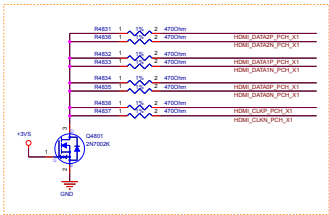
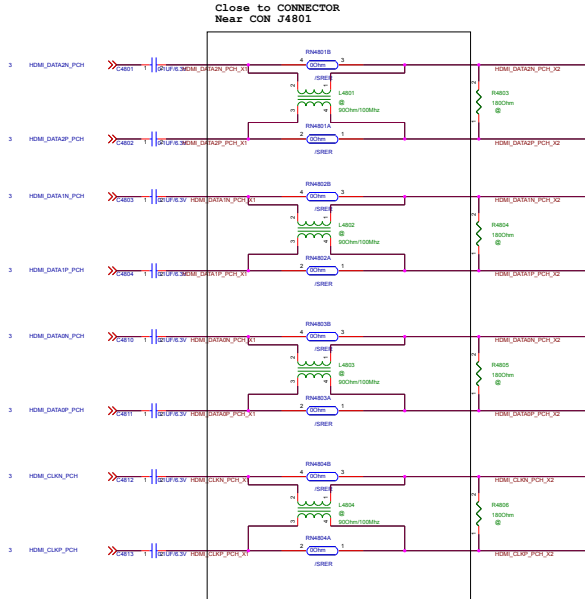
Camera +3V3_CAM Power



Touch



HDMI type-A

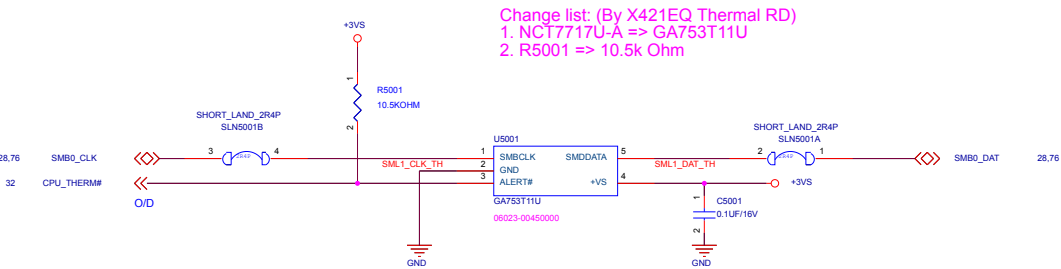


0306 EMI request
SWAP

0331 Change U4802 U4803 PN 07024-01950200
EMI request

request

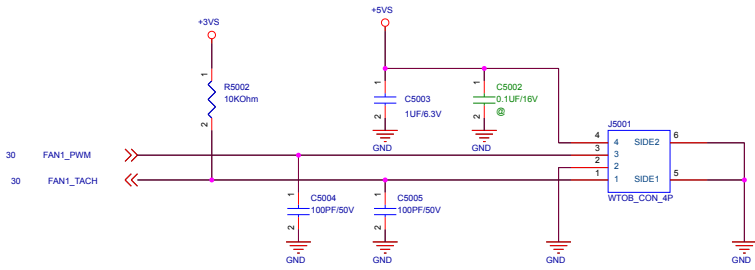
CPU Thermal Sensor

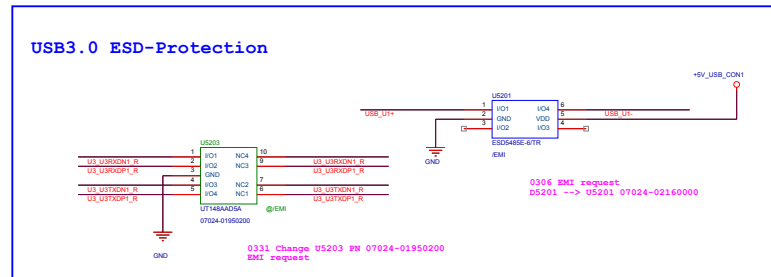


ALERT# point hardware power-on setting
The default value could be set after power up 100ms
by different pull-up resistor of ALERT# pin:

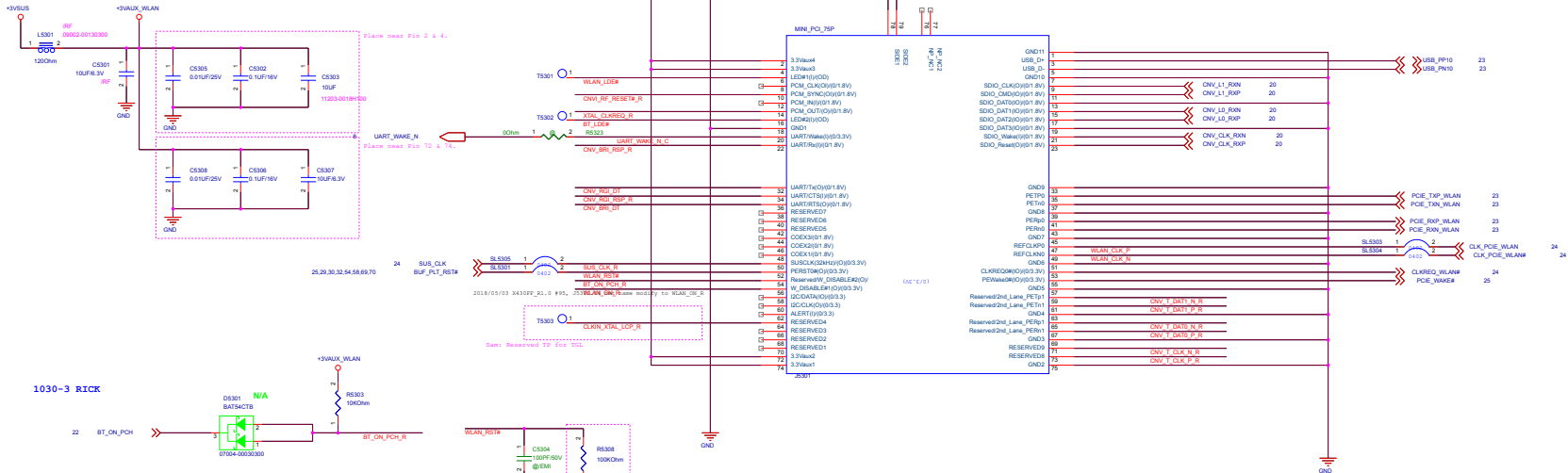
PULL-UP RESISTOR	TEMPERATURE (°C)
2kΩ	75
7.5kΩ	90
10.5kΩ	100
14kΩ	105
18.7kΩ	110

DC FAN Control

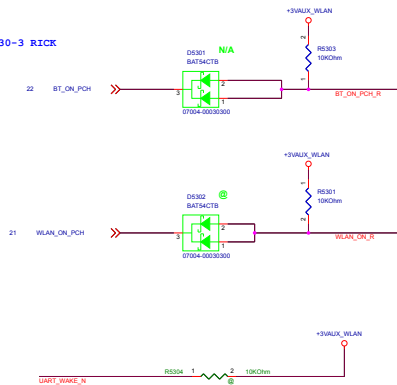




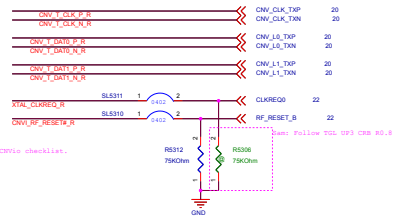
Support PCIE/CNVi co-lay



1030-3 RICK



GPP_B2 for CNVI BT UART WAKE:



San: Follow TGL UP3 CMB R0.8

[请靠近Conn](#)

Sam: Follow 575882 CNVio checklist

36.3.2.4 AC Capacitor General Guidelines for M.2 SSD Storage Routing on SATA / PCI Express* Multiplexed Ports

The following table summarizes the AC capacitor requirements on the motherboard when using the SATA/PCIe* multiplexed ports.

Note:

When SATA and PCIe* are muxed, always route according to SATA design guidelines. SATA does not support signal polarity reversal and does not support lane reversal.

Table 36-7. SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF ²	None	None ³

Notes:

- Design Constraint: For PCIe only application, please refer to the PCIe guidelines for details.
- Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the 10 nF capacitor on nF capacitors can be removed if DC coupled ODDs / devices are NOT used.
- Design Constraint: For PCIe* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
- Design Constraint: For PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
- Design Constraints Required: Refer to Chapter 3, "General Differential Signals Design Guidelines" along with the additional guidelines in this section for all design optimization guidelines.
- Design Constraint: For PCIe* lanes that needs to support either **PCIe* Gen2 devices** or **PCIe* Gen3 devices**, follow the PCIe* Gen 3/ SATA multiplexed configuration where the motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**

6.2.2 PLN Pin Update for M.2 Based NVMe* Storage

A new optional pin (Pin 8) in M.2 pinout, called PLN, has been defined to provide the NVMe* SSD an early warning that power will be lost on long power button press. This allows the SSD to prepare as if a graceful shutdown and avoid unexpected power loss.

Customers are advised to have this additional pin connected per below:

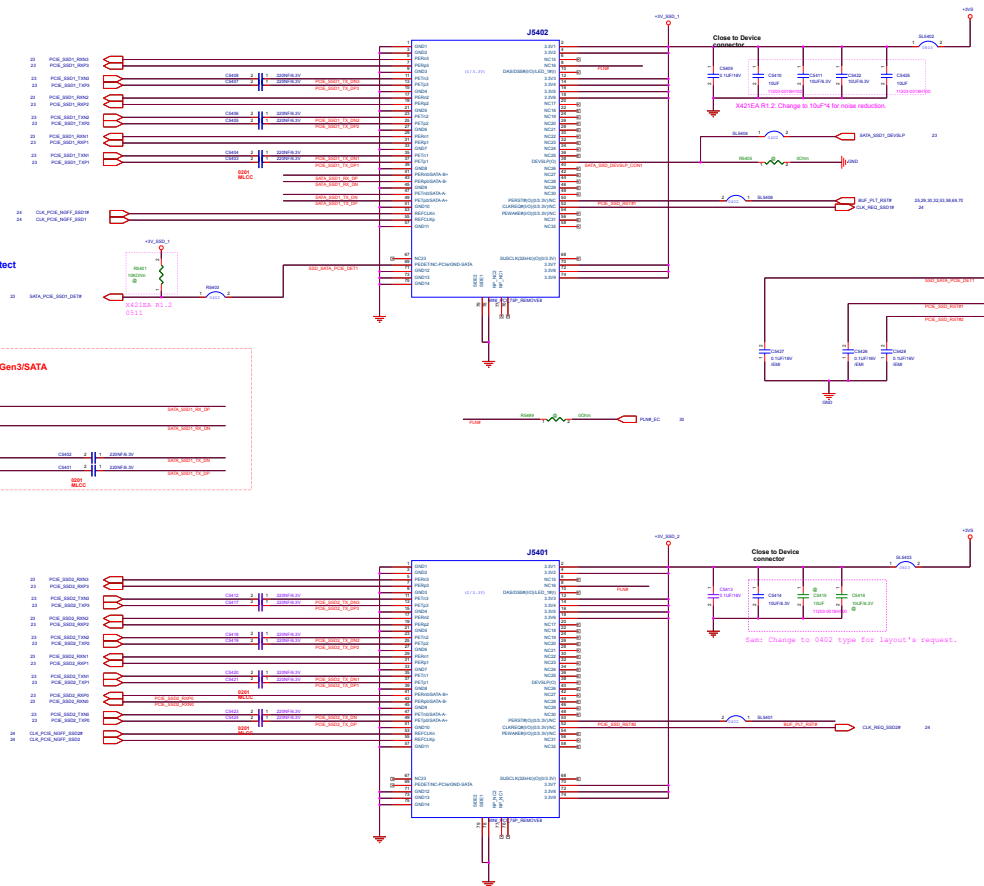
- If customer design is using EC Controller, the power button is routed to EC Controller and EC Controller GPIO is routed to Pin 8 of M.2 connector.
- If customer design is using a discrete solution, the power button should route to a logic controller with the output going into Pin 8 of the M.2. An additional GPIO from PCH to the discrete controller is needed to output a low or high depending on button press length.

For more details on the usage and connectivity of PLN pin, refer to the PLN section of upcoming PDG Rev 1.0 (~W088)

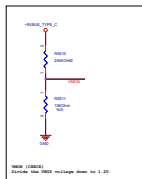
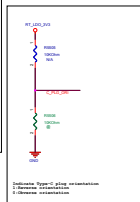
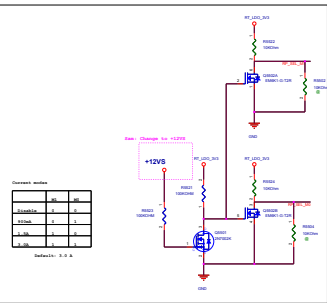
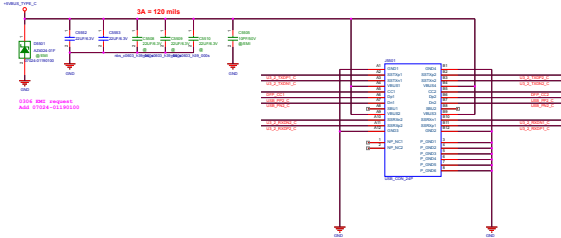
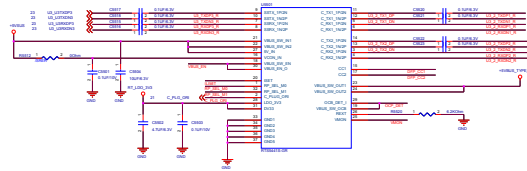
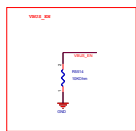
For PCIe/SATA Auto Detect

M.2 SSD Pin Definition
PCIe: M.2-1
SATA: M.2-8

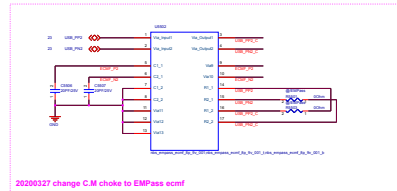
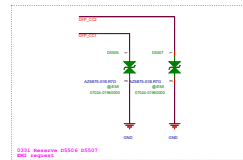
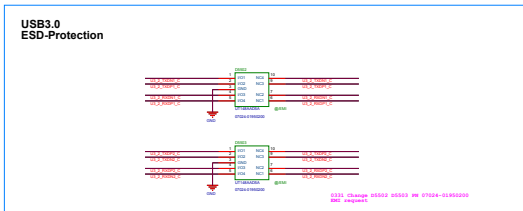
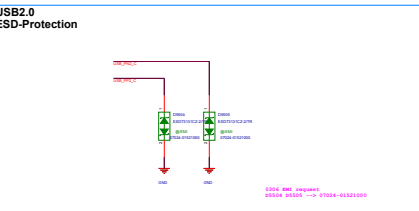
Default PCIe Gen3/SATA Multiplexed



Customer Name:

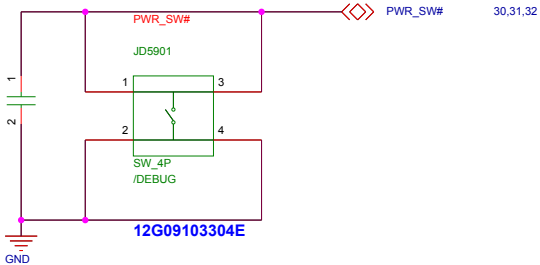


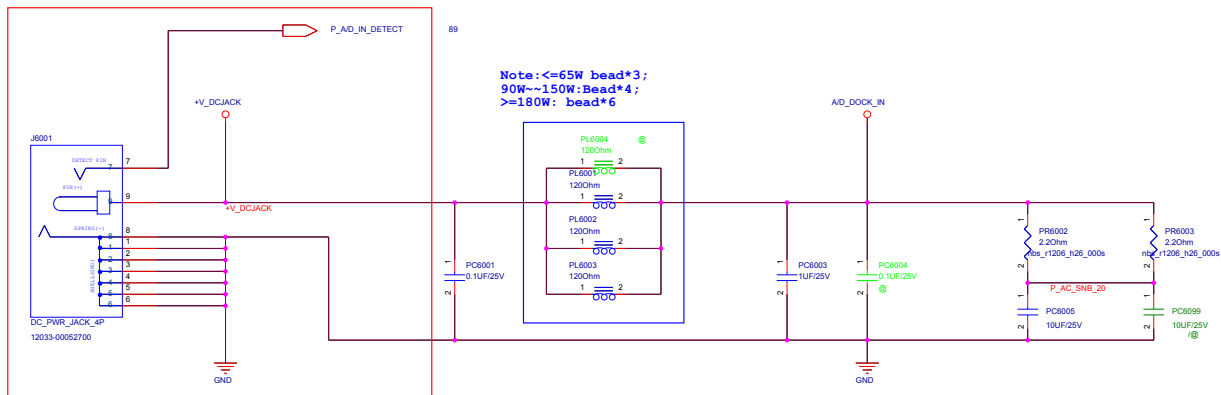
EM PASS 09022-0010000
COP-001
100302000004030 RES A 0 OHM(0402)JUMP 2K4P1YAGE0



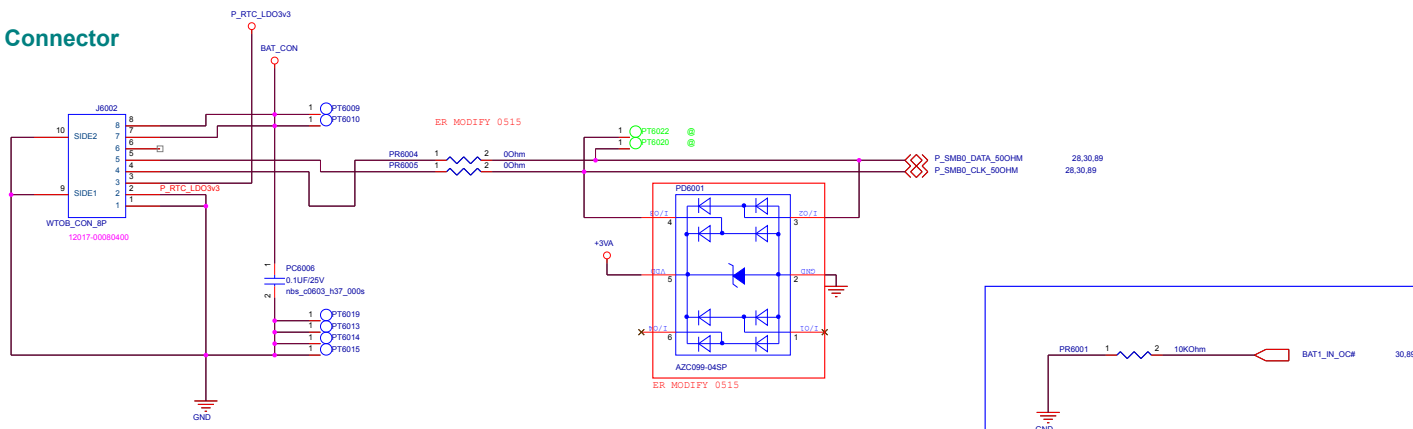


C5902
0.1UF/16V
/DEBUG

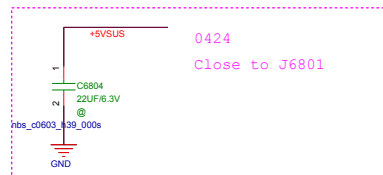
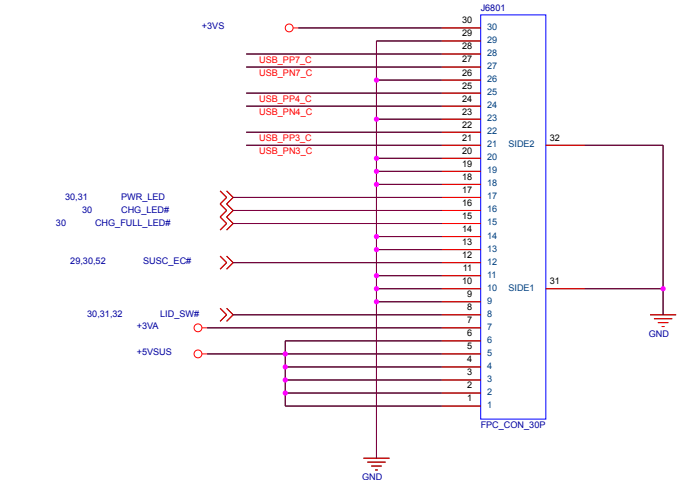
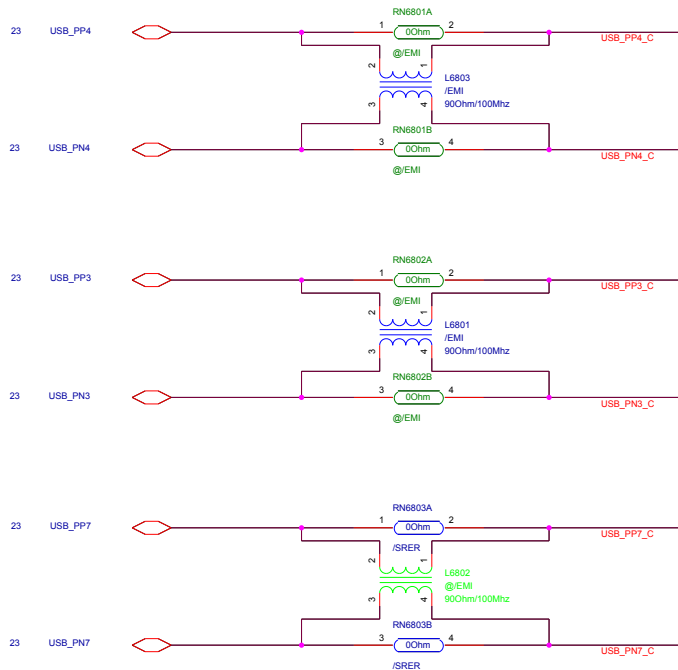




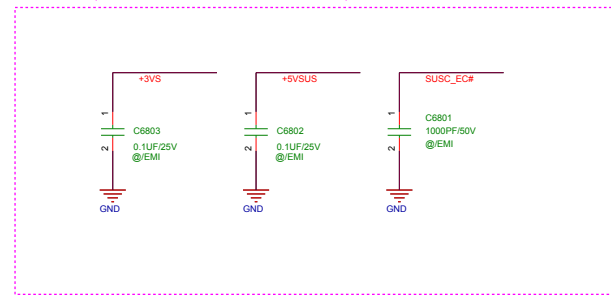
Battery Connector



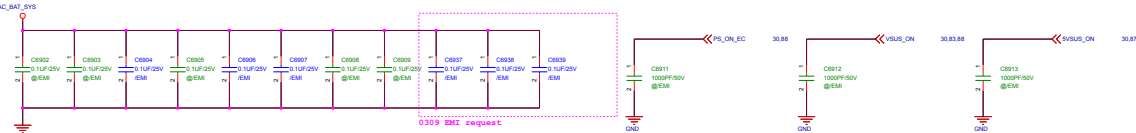
Reference from UX393 and UX350
BAT1 IN OC# Pull down 10K to GND



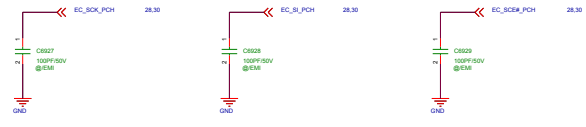
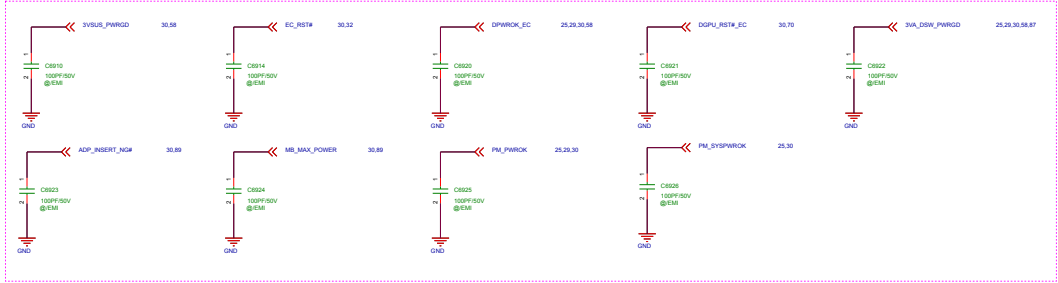
EMI (Close to J6801)



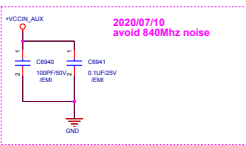
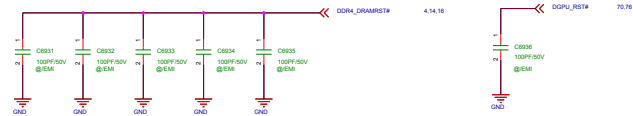
EMI



Close to EC U3001



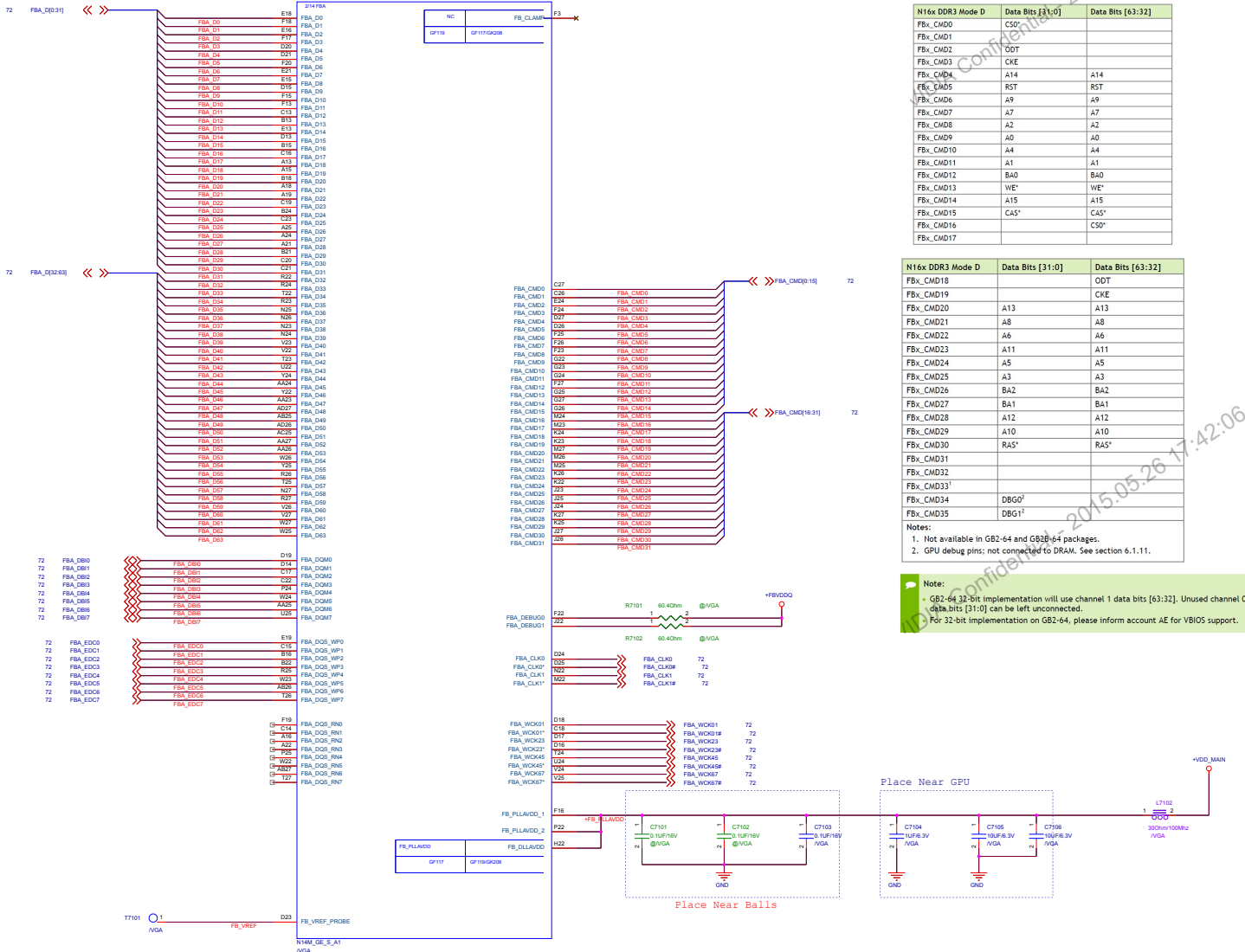
Close to CPU U0301





23	PCIEG_RXFP3[0]	
23	PCIEG_RXFP3[0]	
23	PCIEG_RXFP3[0]	
23	PCIEG_RXFP3[0]	



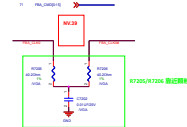


FBA Partition Memory (1 of 2)

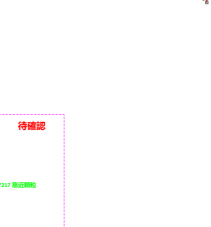
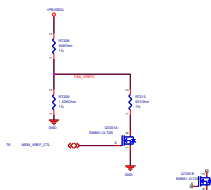
MF=0 Normal

GDD5 MODE SELECTION

MODE	MF	EDCS	EDCS
00	0	VDDQ	VDDQ
01	0	VDDQ	VDDQ
x16 mirrored	VDDQ	VDDQ	0
x32 mirrored	VDDQ	VDDQ	VDDQ



待確認

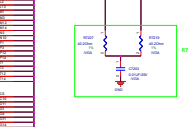


FBA Partition Memory (2 of 2)

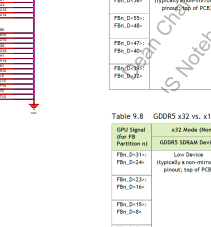
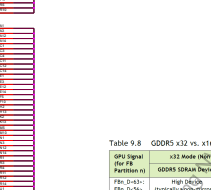
MF=0 Normal

GDD5 MODE SELECTION

MODE	MF	EDCS	EDCS
00	0	VDDQ	VDDQ
01	0	VDDQ	VDDQ
x16 mirrored	VDDQ	VDDQ	0
x32 mirrored	VDDQ	VDDQ	VDDQ



待確認



USE GDDR5 VRAM 16GB x 32 (16GB)
1st: P/N: 83008-0000000 MICRONMT81J256M2HF-70A (A-die), Strap: 6x1 (+1.35V)
2nd: P/N: 83008-0000000 SAMSUNGK4G6132FB-HC10 (B-die), Strap: 6x1 (+1.35V)

+1.35V
+1.35V

待確認

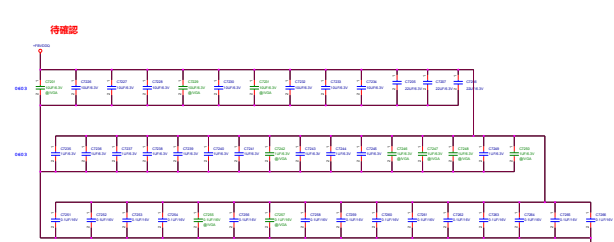


Table 9.18 GPU-Side FBVDDQ Decoupling Requirements

Decoupling Capacitor		Recommended Quantity and Placement (for all supported partitions combined)	
Capacitance	Type Size	Quantity	Placement
For N17x GPU Package: GB2C-64 (preliminary)			
1.0 uF	X65 [0402]	8	Under GPU FBVDDQ ball (evenly distributed throughout partition)
10 uF	X65 [0603]	2	
10 uF	X65 [0603]	1	Near GPU device
22 uF	X65 T60631	3	

Table 9.19 DRAM-Side FBVDDQ/FBVDDQ Decoupling (Combined Ref)

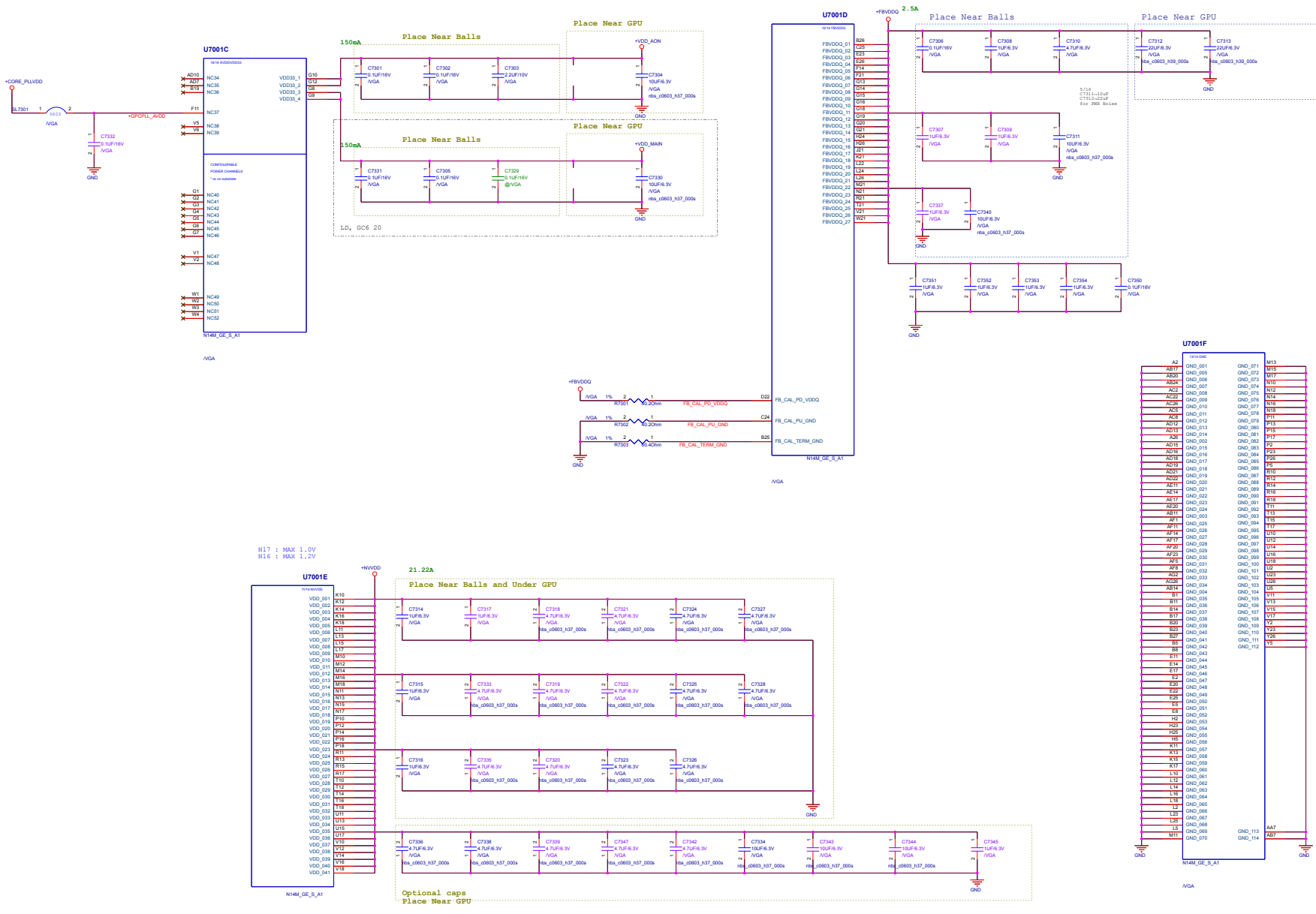
Decoupling Capacitors		Recommended Quantity and Placement (per DRAM device)	
Capacitance	Type [Size]	Quantity	Placement (by DRAM/Interface Node)
Combined FBVDDQ/FBVDQ rail			
1.0 uF	X65 [0402]	16	For x32 DRAM: Under the DRAM FBVDDQ or FBVDQ ball. For x16 DRAM: In a "clamsHELL" PCB configuration: As close to DRAM periphery as possible.
10 uF	X65 [0603]	2	Ensure at least 2 GND vias and 2 power vias for each capacitor.
1.0 uF	X65 [0402]	8 additional	For x32 DRAM: Choose x32 interface to achieve max PCB drain speeds. Add these additional decoupling caps under the DRAM FBVDDQ ball; should share existing FBVDDQ-Q ball via if possible. See Figure 9.23 for an example.
10 uF	X65 [0603]	2	Near DRAM device. Ensure at least 2 GND vias and 2 power vias for each capacitor.
22 uF	X65 [0603]	3	For 4 GHz WCK (3 Gbps data rates): Near DRAM device. Ensure at least 2 GND vias and 2 power vias for each capacitor.

Table 9.8 GDDR5 x32 vs. x16 Data Bus Connectivity

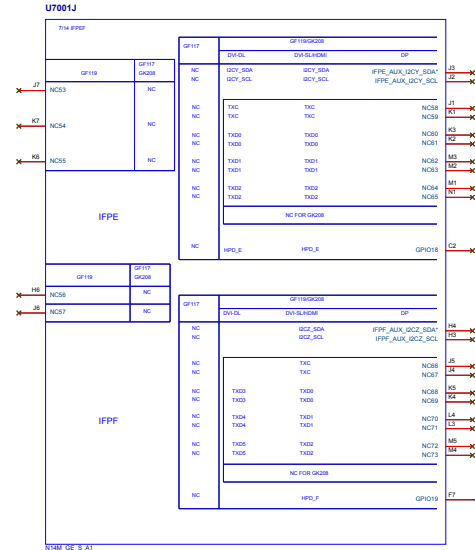
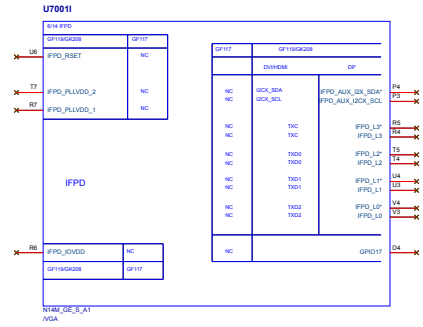
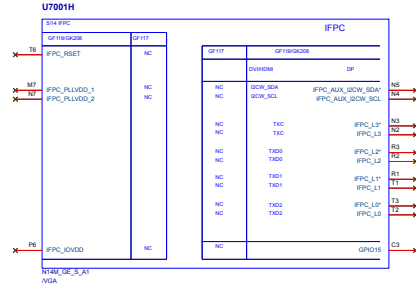
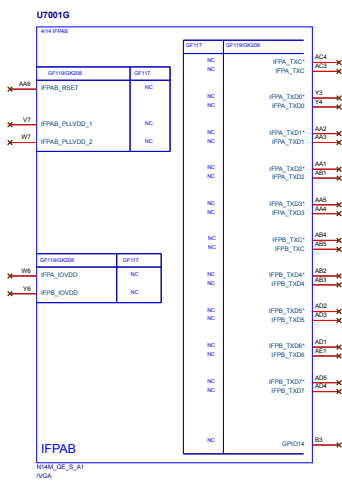
GPU Signal (for FB Partition n)	x32 Mode (Non-Clamshell)	x16 Mode (Clamshell)		
	GDDR5 SDRAM Device	Data Lines	GDDR5 SDRAM Device	Data Line
FBn_D-63+/- FBn_D-35+/-	High Diego (typically x16-mirrored pinout; top of PCB)	DQ17:DQ24	HI-CH Mem Device 1 (mirrored pinout; bottom of PCB)	DQ31:DQ24
FBn_D-35+/- FBn_D-48+/-		DQ25:DQ16	HI-CH Mem Device 0 (non-mirrored pinout; top of PCB)	DQ31:DQ16
FBn_D-47+/- FBn_D-40+/-		DQ15:DQ8	HI-CH Mem Device 1 (mirrored pinout; bottom of PCB)	DQ15:DQ8
FBn_D-7+/- FBn_D-0+/-		DQ7:DQ0	HI-CH Mem Device 0 (non-mirrored pinout; top of PCB)	DQ7:DQ0

Table 9.8 GDDR5 x32 vs. x16 Data Bus Connectivity (Continued)

GPU Signal (for FB Partition n)	x32 Mode (Non-Clamshell)		x16 Mode (Clamshell)	
	GDDR5 SDRAM Device	Data Lines	GDDR5 SDRAM Device	Data Lines
FbIn_D-31+/- FbIn_D-24+/- FbIn_D-15+/- FbIn_D-8+/- FbIn_D-7+/- FbIn_D-0+/-	Low Device (typically a non-mirrored pinout; top of PCB)	DQ31:DQ24	Low-CH Mem Device 1 (mirrored pinout; bottom of PCB)	DQ31:DQ24
		DQ23:DQ16	Low-CH Mem Device 0 (non mirrored pinout; top of PCB)	DQ31:DQ16
		DQ15:DQ8	Low-CH Mem Device 1 (mirrored pinout; bottom of PCB)	DQ15:DQ8
		DQ7:DQ0	Low-CH Mem Device 0 (non mirrored pinout; top of PCB)	DQ7:DQ0



LVDS



CRT

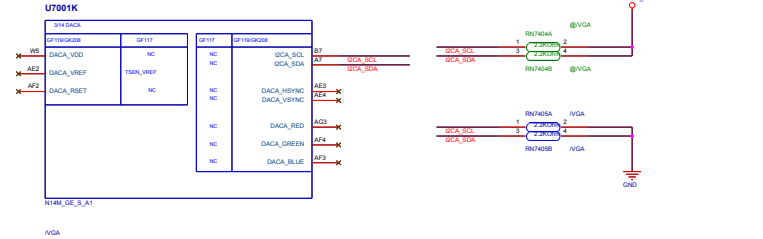


Table 5.5 SORx_EXPOSED Enablement for Down Designs

Row Index	Strap Pins see Note			Resulting SORx_EXPOSED Enablements			
	ROM_SQ	ROM_SI	ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	H	ENABLED	ENABLED	disabled	disabled
13	L	H	L	ENABLED	ENABLED	disabled	ENABLED
12	L	H	H	ENABLED	ENABLED	disabled	disabled
8	H	H	H	ENABLED	disabled	disabled	disabled
0	H	H	M	disabled	disabled	disabled	disabled
	M	X	X	(Reserved; do not configure)			
	All other Strap Configurations			(Reserved)			

Table 5.3 RAMCFG

Strap Pins see Note			RAMCFG Setting Number (see Memory RVL for memory configs corresponding to these numbers)
STRAP2	STRAP1	STRAP0	
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	H	L	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

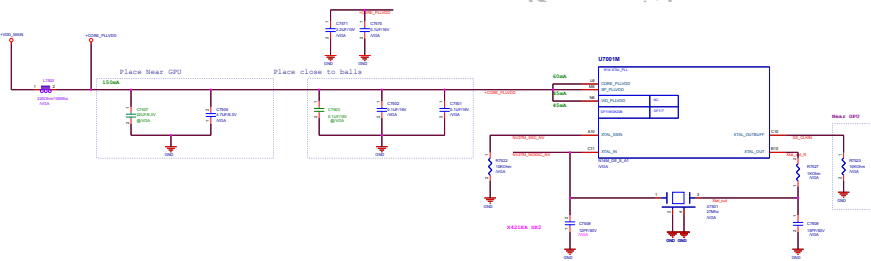
Table 4. N175-G5/LP GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32 512Mx16	1.35V	Micron	MT51J256M32HF-80:B	B-die	0x9	8 Gbps	N/A	Full	Production candidate
			Hynix	H5GC8H24JR-R2C	A-die	0xA	8 Gbps	N/A	Full	Production candidate
			Samsung	K4G80325FC-HC25	C-die	0xB	8 Gbps	N/A	Full	Production candidate

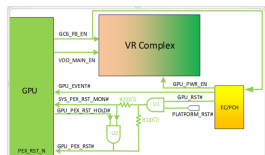
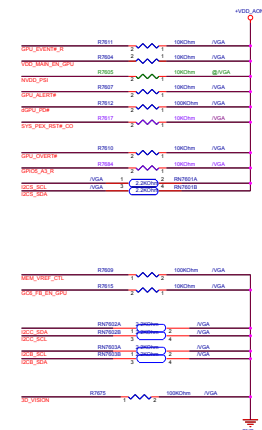
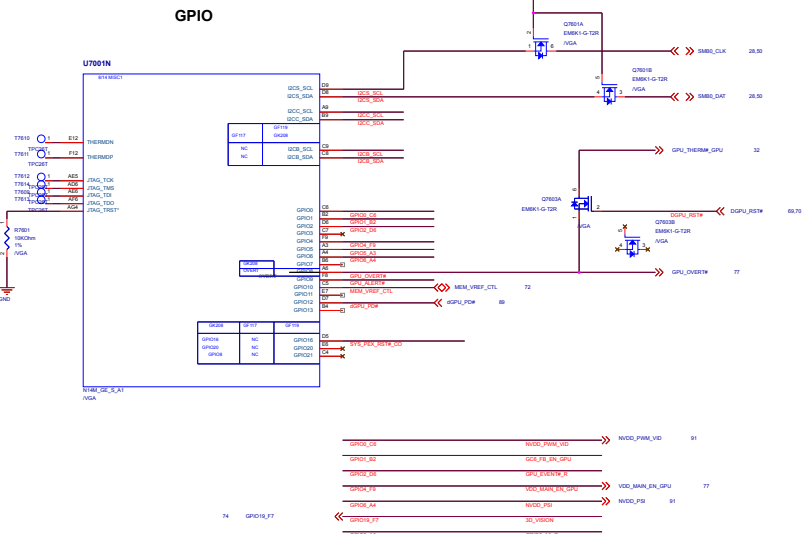
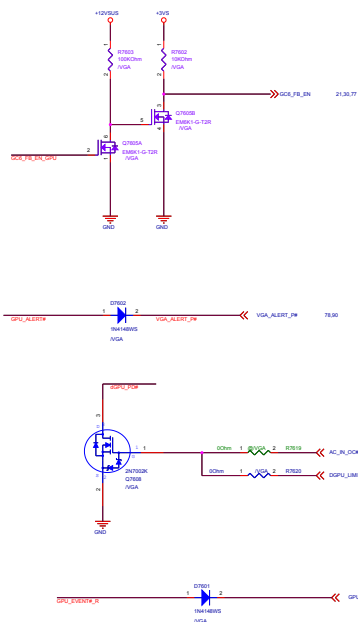
Notes:

- For N175-G5/LP, the maximum allowable memory case temperature is 85 °C.

Xtal

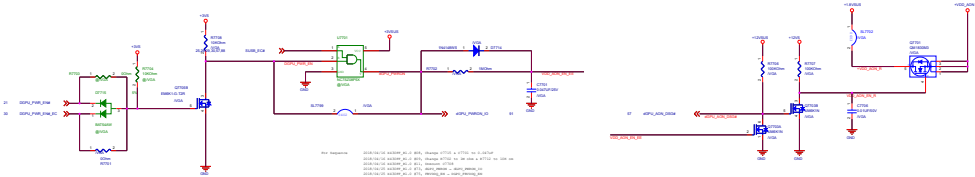


Level shift
N17:1.8V
N16:3.3V

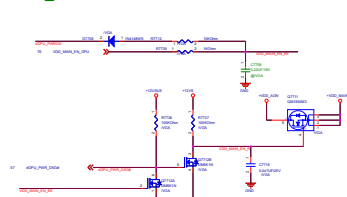


1. +VDD_AON
N17 : 1.8V
N16 : 3.3V

dgPU Power Sequence

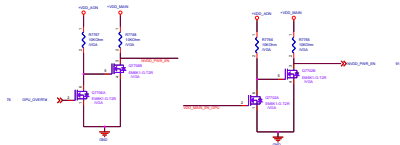


2. +VDD_MAIN



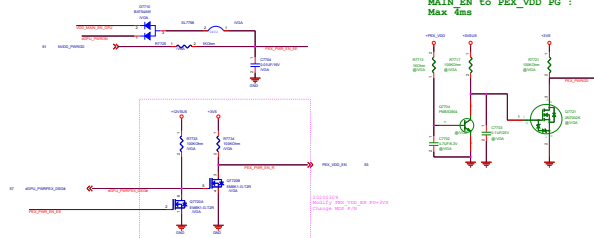
3. NVDD EN

VENH : Min 1.2V
EN high to PGOOD : 2.5ms

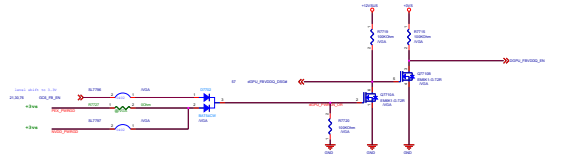


4. +PEX

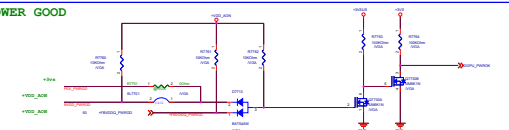
MAIN_EN to PEX_VDD PG :
Max 4ms



5. +FBVDD EN



6. GPU POWER GOOD



N17X-PWR SEQ

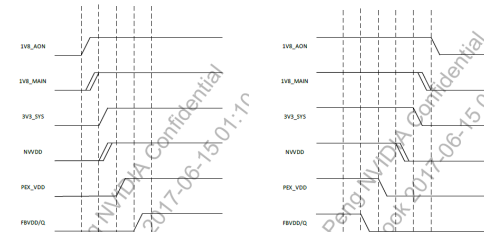


Figure 5. H17/G82C-64 GPU Power-Up Sequencing

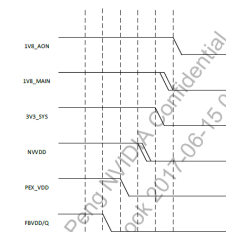
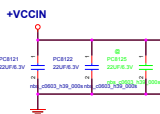
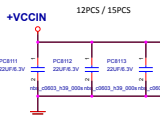
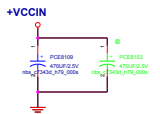
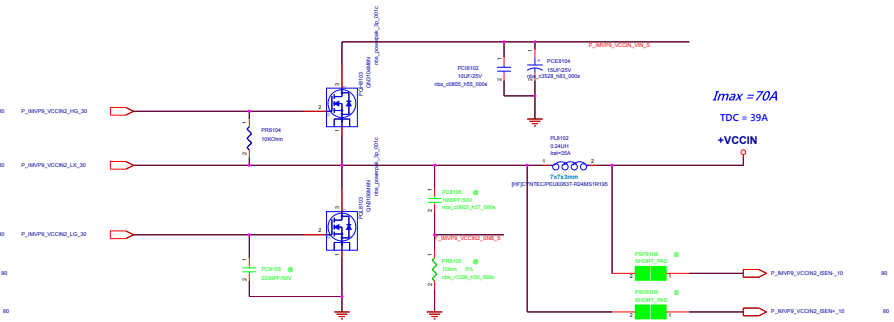
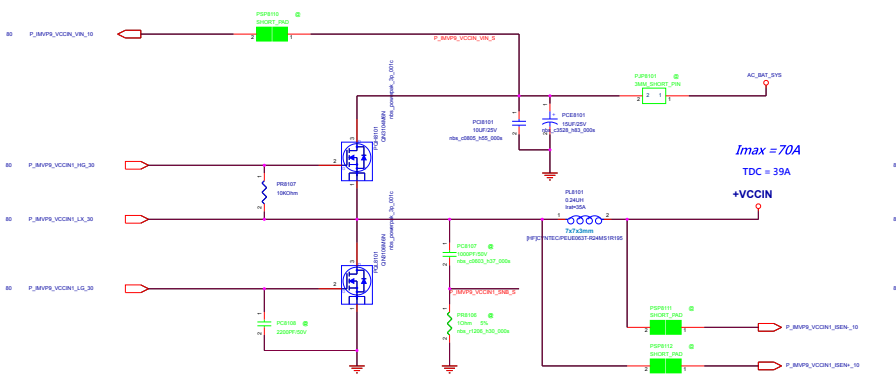
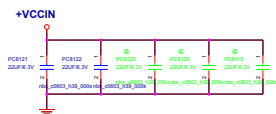
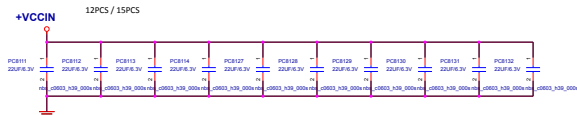


Figure 6. H17/G82C-64 GPU Power-Down Sequencing

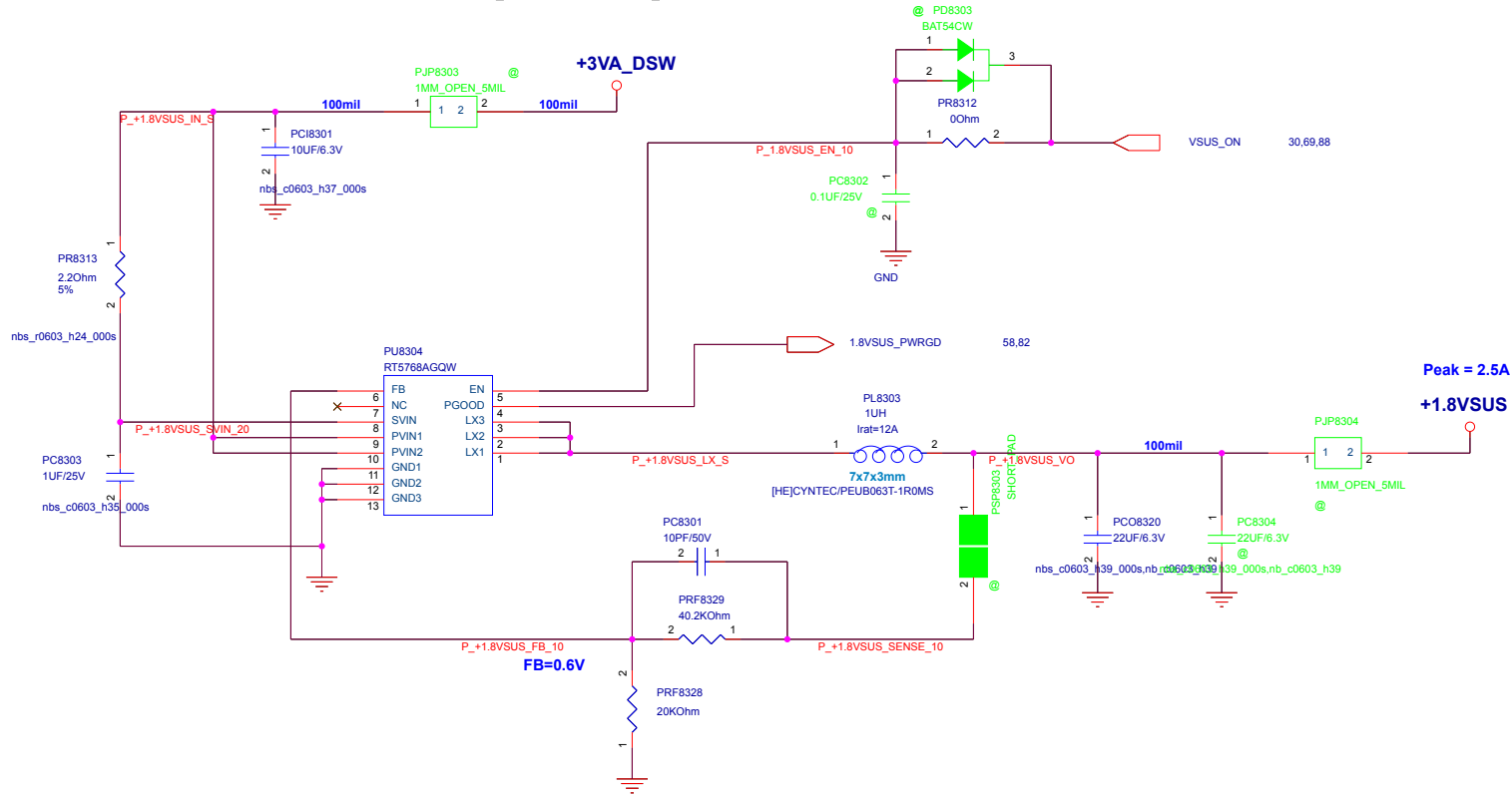


輸出電容組合

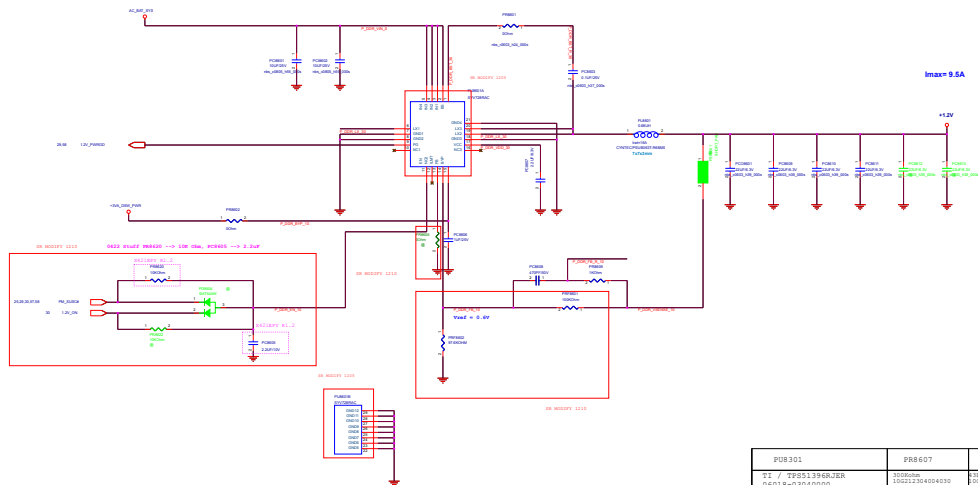
POSICAP	MLCC
3.30uF / 2.5V	22uF / 6.3V
1PCS	12PCS
2PCS	4PCS



+1.8VSUS [For PCH]

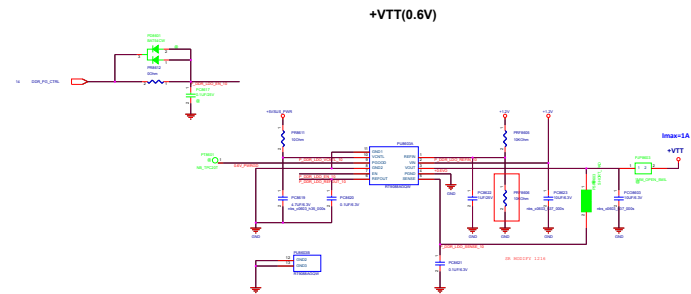
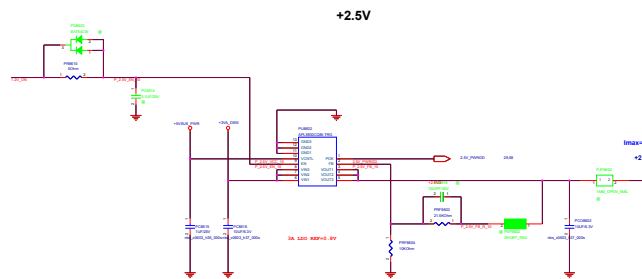


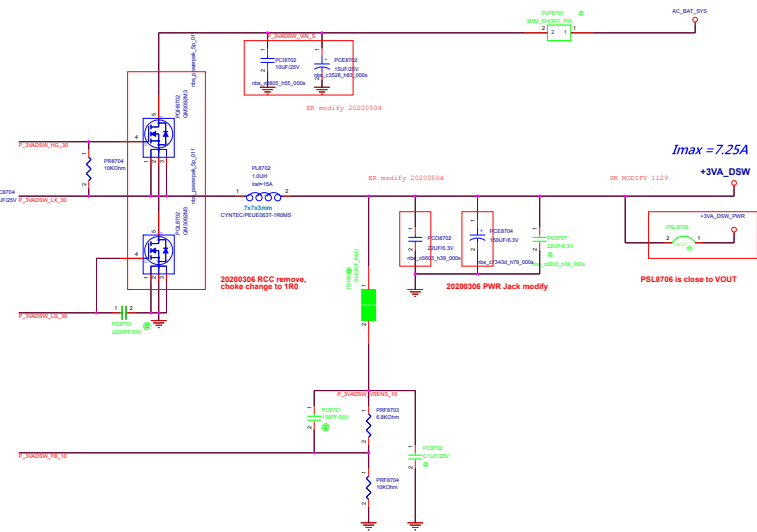
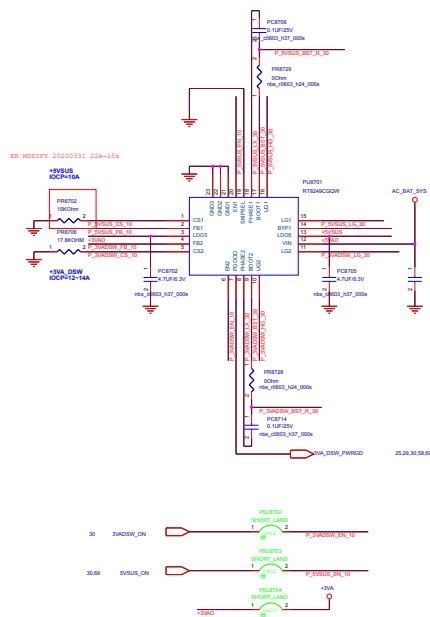
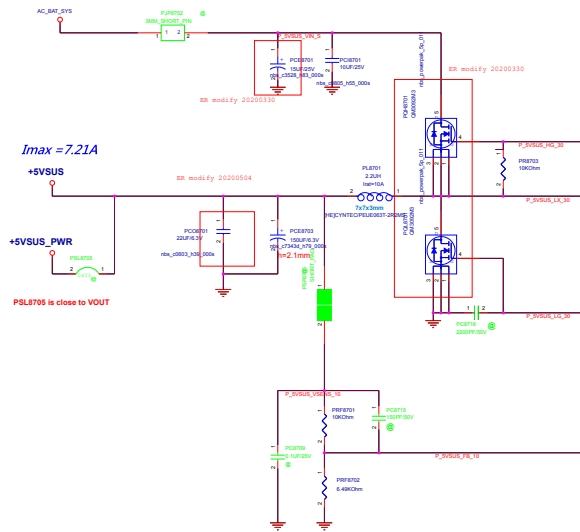
+1.2V [For DDR]



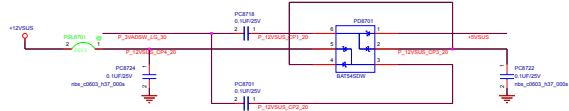
FCR301	FCR607	FCR608	FCR606	FCR604	FCR605	FCR602	FCR603
T1 / TFS1394JEN 06010-33040000	00000000000000000000 09017304004030	00000000000000000000 09017430144010	00000000000000000000 09012000000410	00000000000000000000 09012000000410	00000000000000000000 09012000000410	00000000000000000000 09012000000410	0.01097290 0901010101010030
Slavery / SVT28AC 06010-02930000	0	0	0	0	0	0	0

Current LIMIT自行調整





請 check 整份線路 +12VSUS total 並聯對地電阻不得小於10kOhm



Adaptor Mode (IMVP8)

	S0	S5	S3	D03	S4	S6	S5 with USB Charger+
PS_ON	1	-	1	-	1	-	1
JVADSW_ON	1	-	1	-	1	-	1
3VSUS_ON	1	-	1	-	0	-	0
5VSUS_ON	1	-	1	-	1	-	1
1.35V_ON	1	-	1	-	0	-	0
SUSC_EC#	1	-	1	-	0	-	0
SUSB_EC#	1	-	0	-	0	-	0

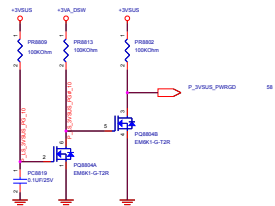
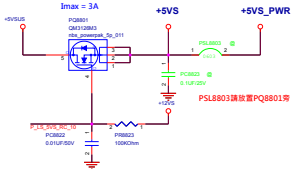
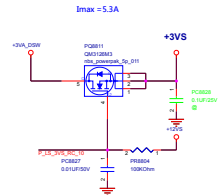
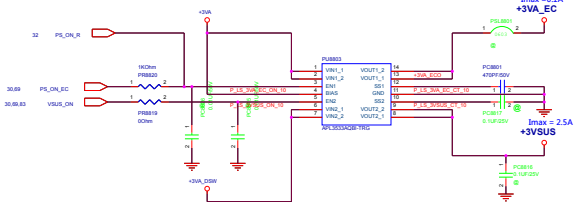
Battery Mode (IMVP8)

	S0	S3	D03	S4	S5	S5 with USB Charger*
PS_ON	1	-	-	1	0	1
3VADSUS_ON	1	-	-	1	0	0
3VSUS_ON	1	-	-	0	0	0
4VSUS_ON	1	-	-	1	0	1
1.35V_ON	1	-	-	1	0	0
SUSC_EC#	1	-	-	0	0	0
SUSB_EC#	1	-	-	0	0	0

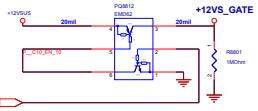
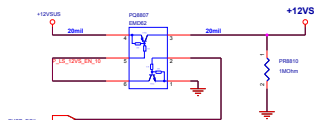
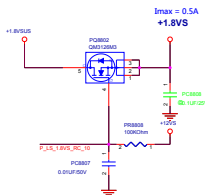
PT870* 請放置 PU8701旁;並請放置Trace 上!

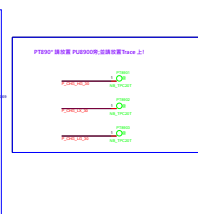
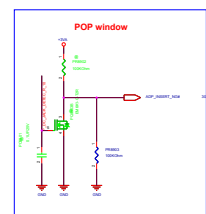
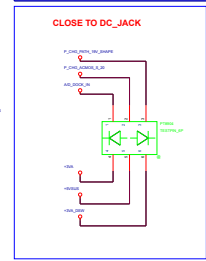
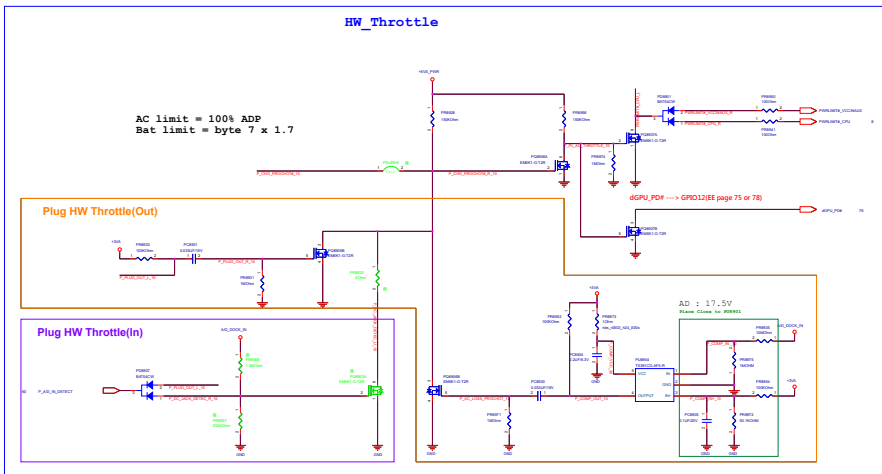
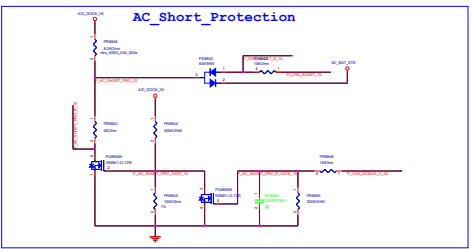
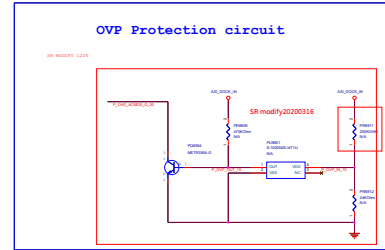
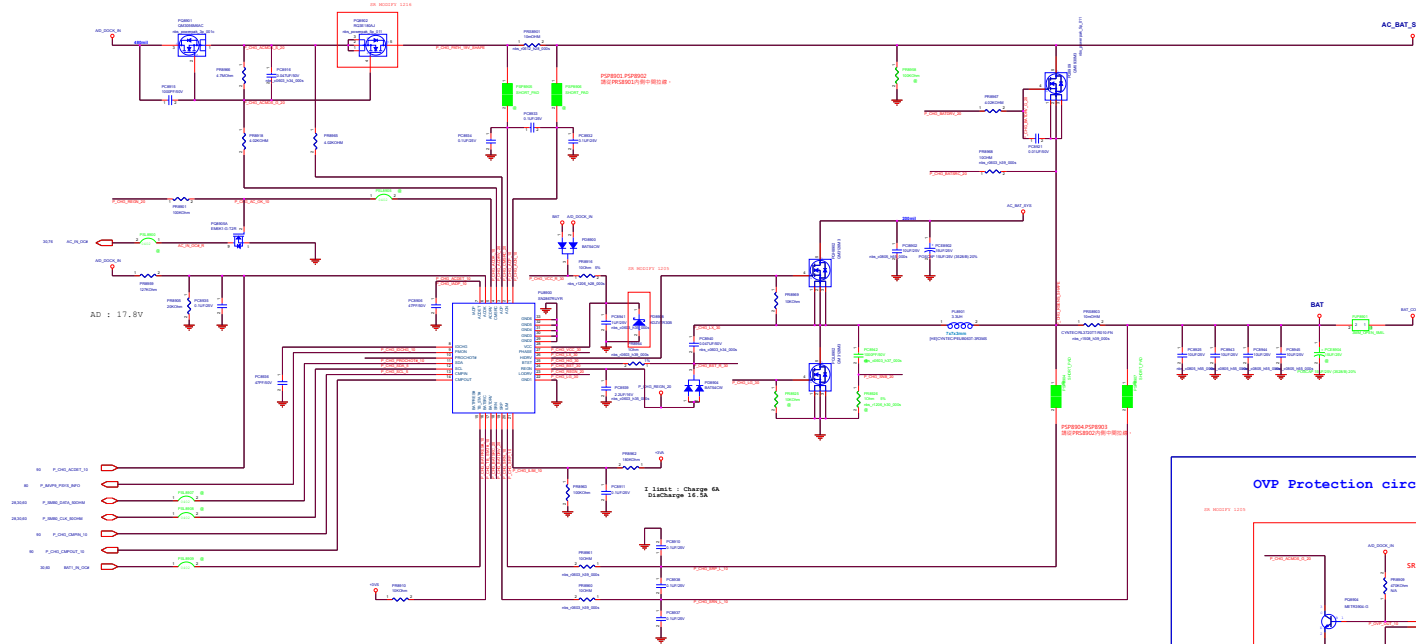


Load Switch



Sam! +VOCFL_OC is integrated in SoC for TGL.



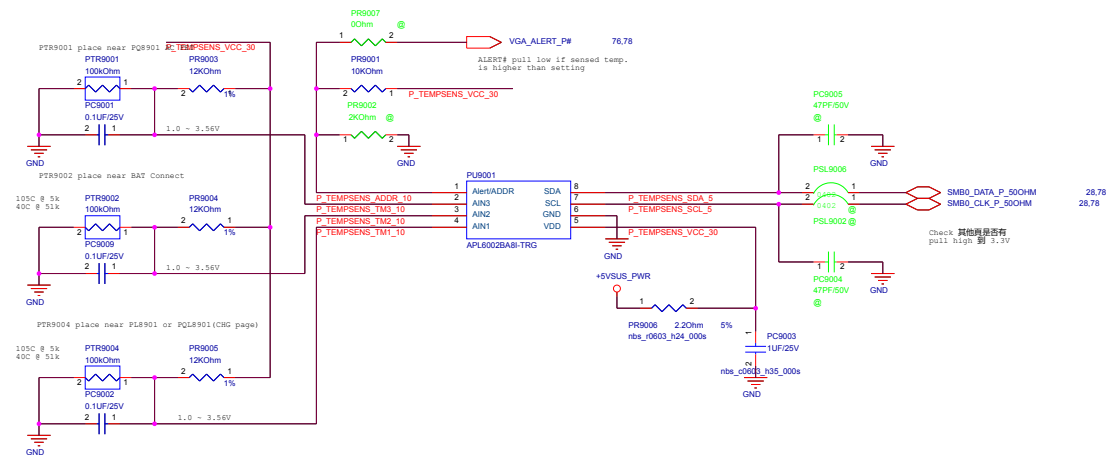


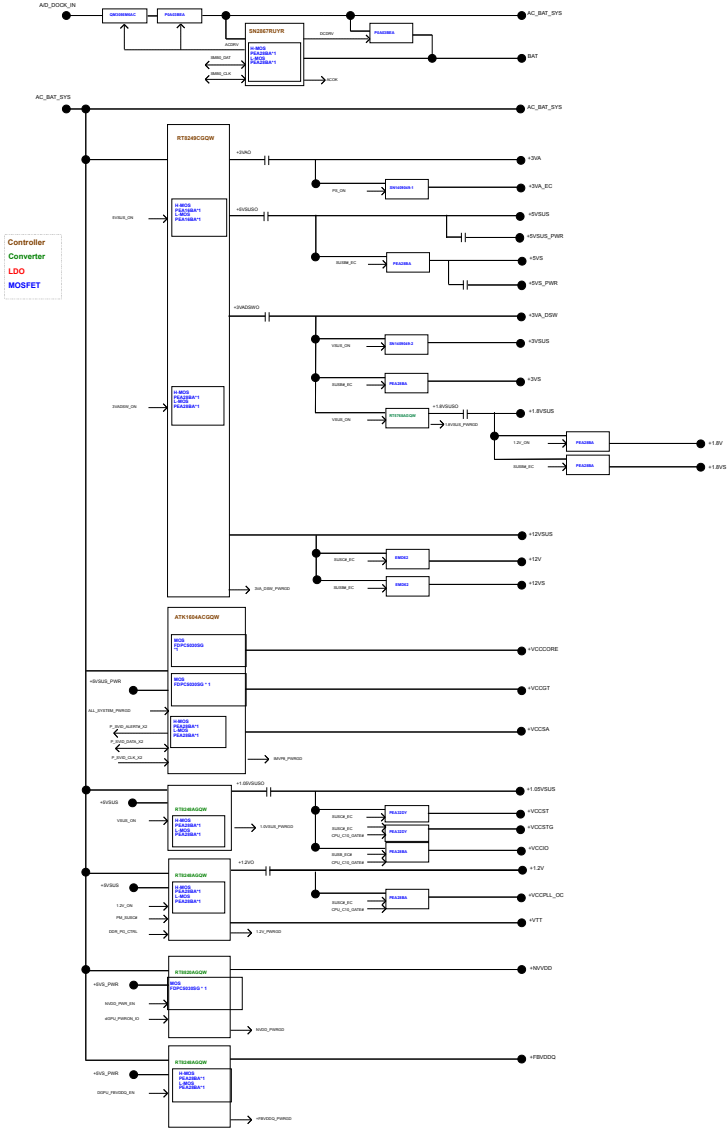
Adaptor select
total power = 90% ADP

Adaptor select		Max. Power	Max. Current
PWR001	3.0A	5A	
PWR002	3.0A	5A	
PWR003	3.0A	5A	
PWR004	3.0A	5A	
PWR005	3.0A	5A	
PWR006	3.0A	5A	
PWR007	3.0A	5A	
PWR008	3.0A	5A	
PWR009	3.0A	5A	
PWR010	3.0A	5A	
PWR011	3.0A	5A	
PWR012	3.0A	5A	
PWR013	3.0A	5A	
PWR014	3.0A	5A	
PWR015	3.0A	5A	
PWR016	3.0A	5A	
PWR017	3.0A	5A	
PWR018	3.0A	5A	
PWR019	3.0A	5A	
PWR020	3.0A	5A	
PWR021	3.0A	5A	
PWR022	3.0A	5A	
PWR023	3.0A	5A	
PWR024	3.0A	5A	
PWR025	3.0A	5A	
PWR026	3.0A	5A	
PWR027	3.0A	5A	
PWR028	3.0A	5A	
PWR029	3.0A	5A	
PWR030	3.0A	5A	
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PWR032	3.0A	5A	
PWR033	3.0A	5A	
PWR034	3.0A	5A	
PWR035	3.0A	5A	
PWR036	3.0A	5A	
PWR037	3.0A	5A	
PWR038	3.0A	5A	
PWR039	3.0A	5A	
PWR040	3.0A	5A	
PWR041	3.0A	5A	
PWR042	3.0A	5A	
PWR043	3.0A	5A	
PWR044	3.0A	5A	
PWR045	3.0A	5A	
PWR046	3.0A	5A	
PWR047	3.0A	5A	
PWR048	3.0A	5A	
PWR049	3.0A	5A	
PWR050	3.0A	5A	
PWR051	3.0A	5A	
PWR052	3.0A	5A	
PWR053	3.0A	5A	
PWR054	3.0A	5A	
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PWR056	3.0A	5A	
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PWR093	3.0A	5A	
PWR094	3.0A	5A	
PWR095	3.0A	5A	
PWR096	3.0A	5A	
PWR097	3.0A	5A	
PWR098	3.0A	5A	
PWR099	3.0A	5A	
PWR100	3.0A	5A	

Address	0x7E	0x7C	0x7A	0x78	0x76	0x74	0x72	0x70
PR9001	10k	1.5k	2k	3.6k	3.9k	4.3k	5.1k	6k
PR9002	Open	8.2k	6.2k	6.8k	4.7k	3.6k	2.7k	2k

Address	0x00 0x01 0x02	0x03 0x04 0x05	0x06
R/W	W W W	R R R	R
Function	Temp. alert threshold setting	Sensed temp. data	bit 4 = 0 bit 5 = 0 bit 6 = 0 When ALERT# assert

[illegible]



Power-On Sequence Timing Diagram Rev.0.1

For Detail power sequence timing spec,
please refer to #543016 chapter 43

